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FIG. 1



"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

2 / 61

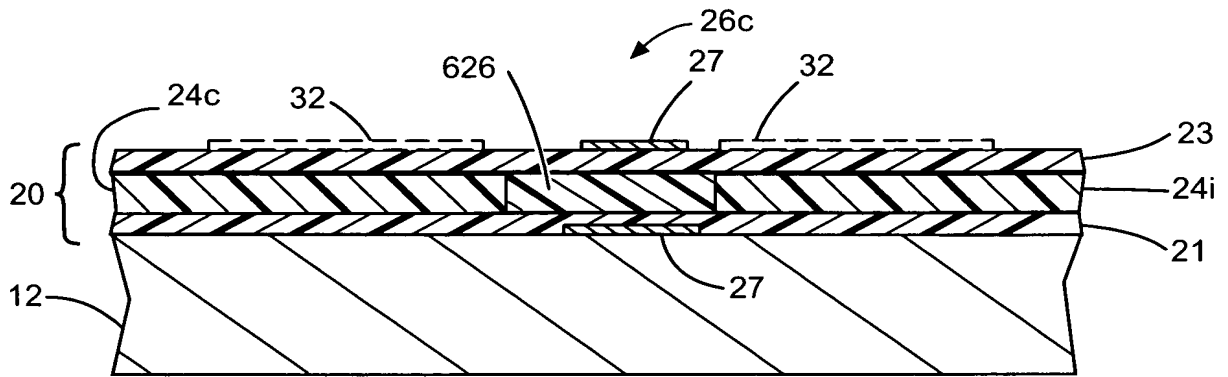


FIG._2

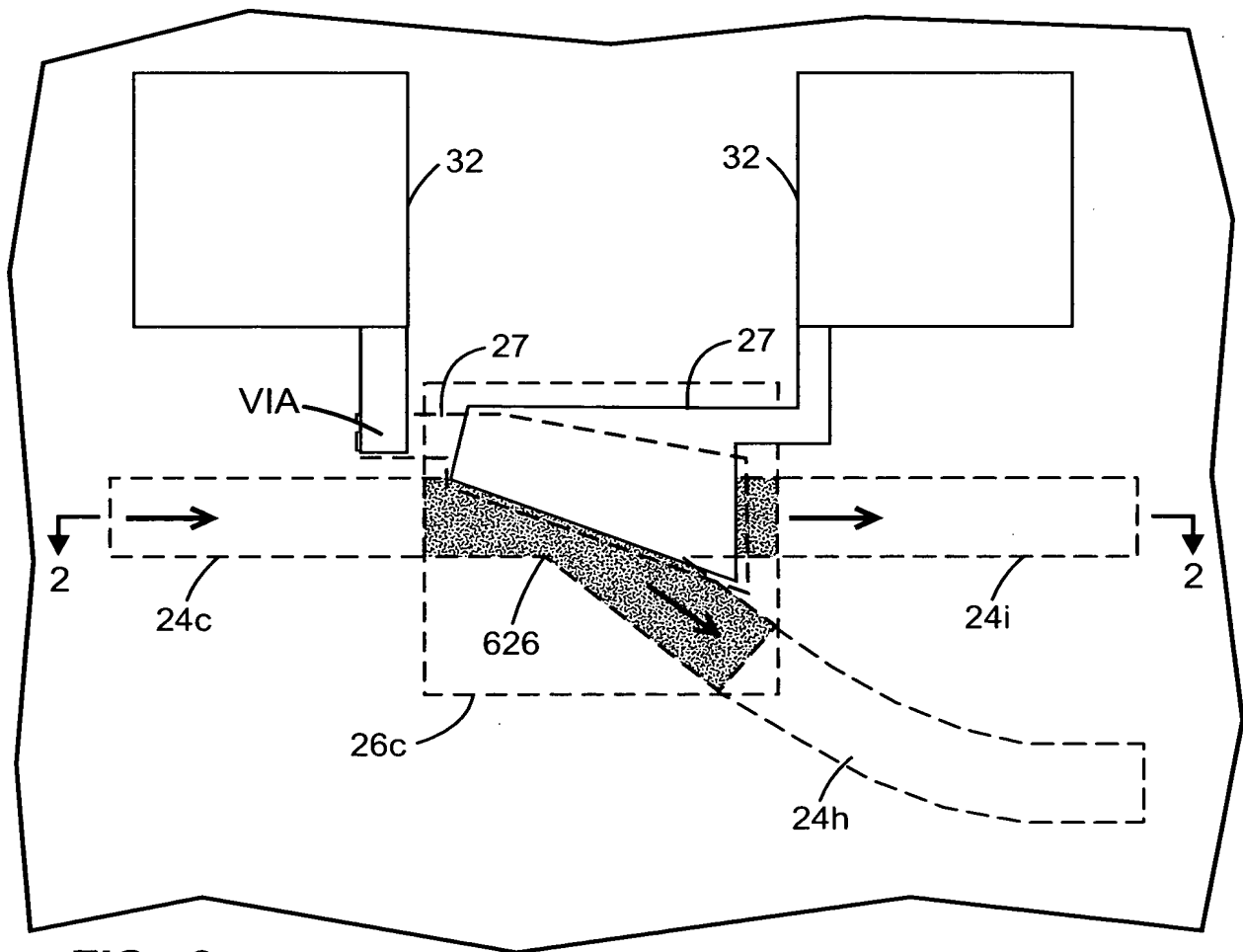


FIG._3



3 / 61

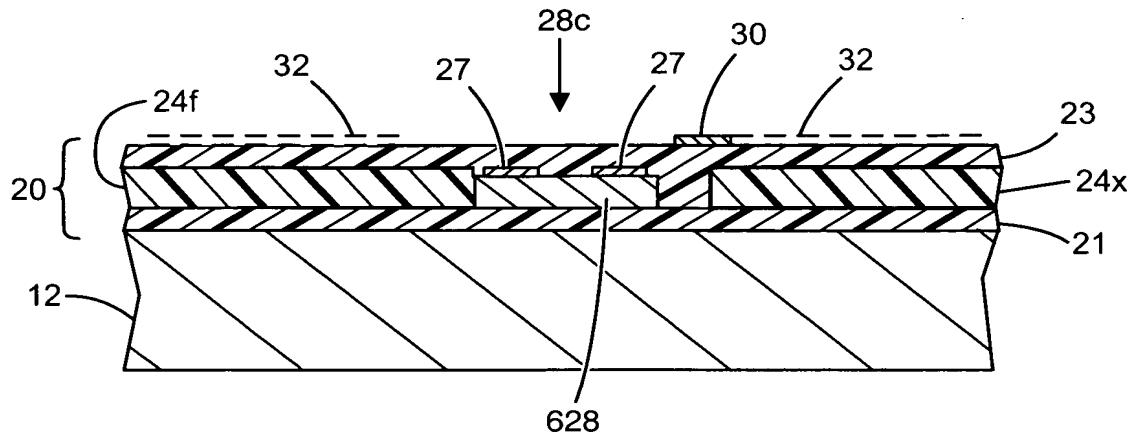


FIG. 4-1

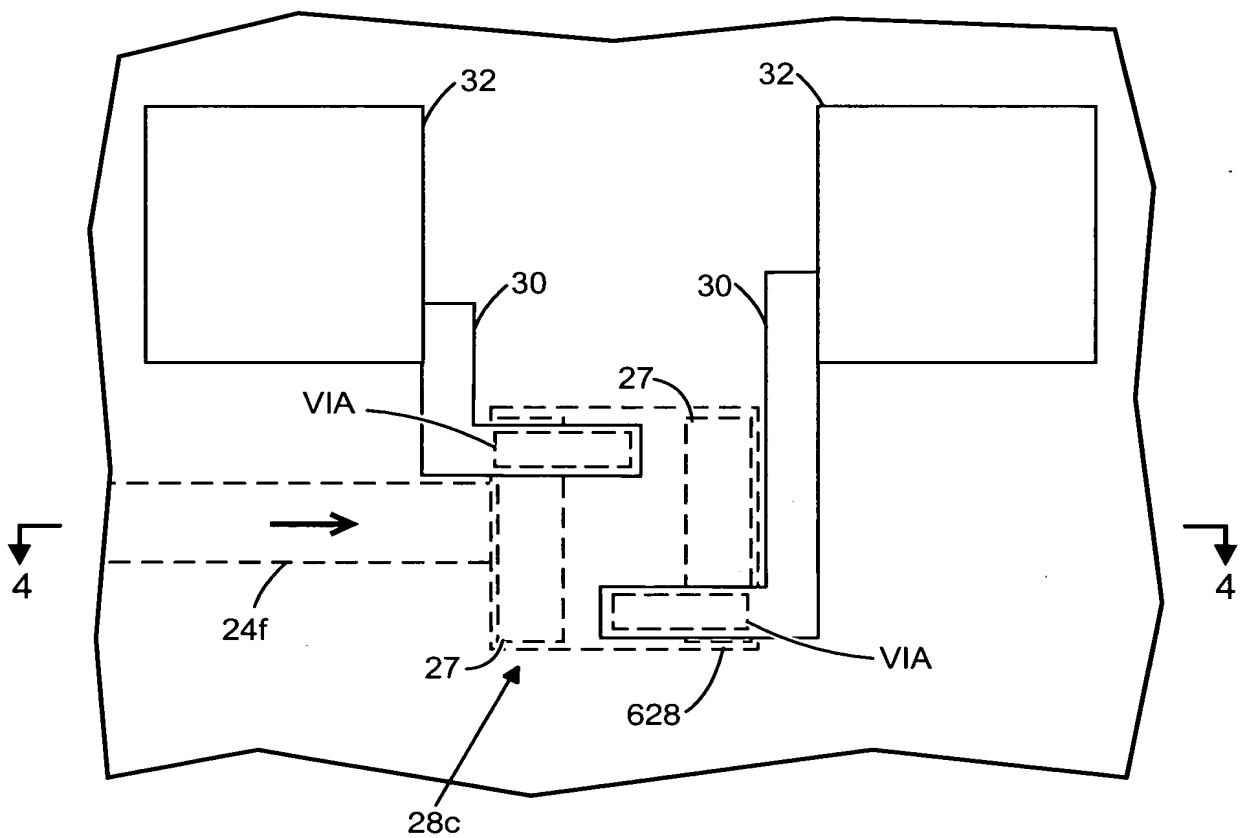


FIG. 5-1



FIG._4-2

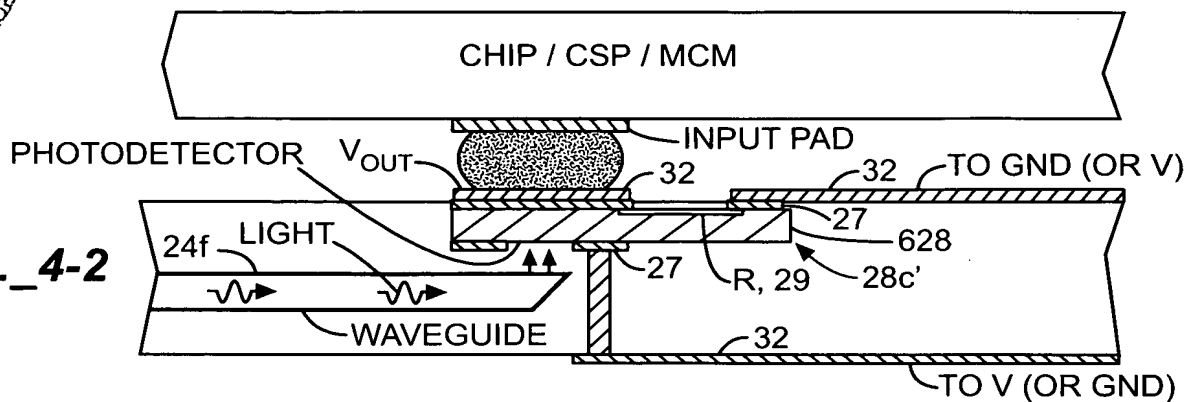


FIG._5-2

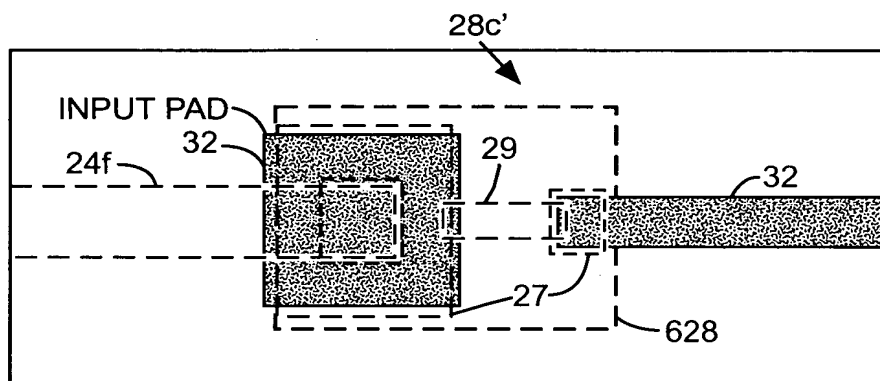


FIG._4-3

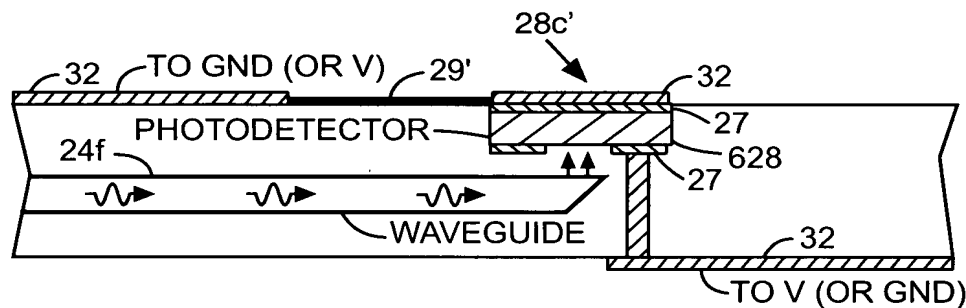
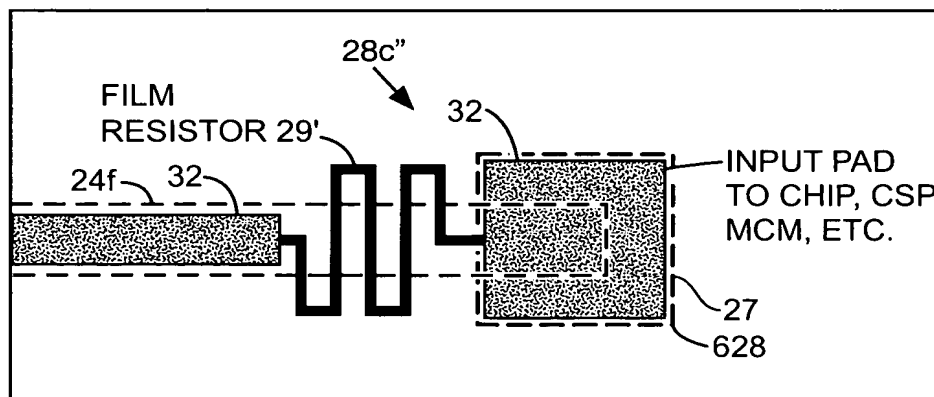


FIG._5-3



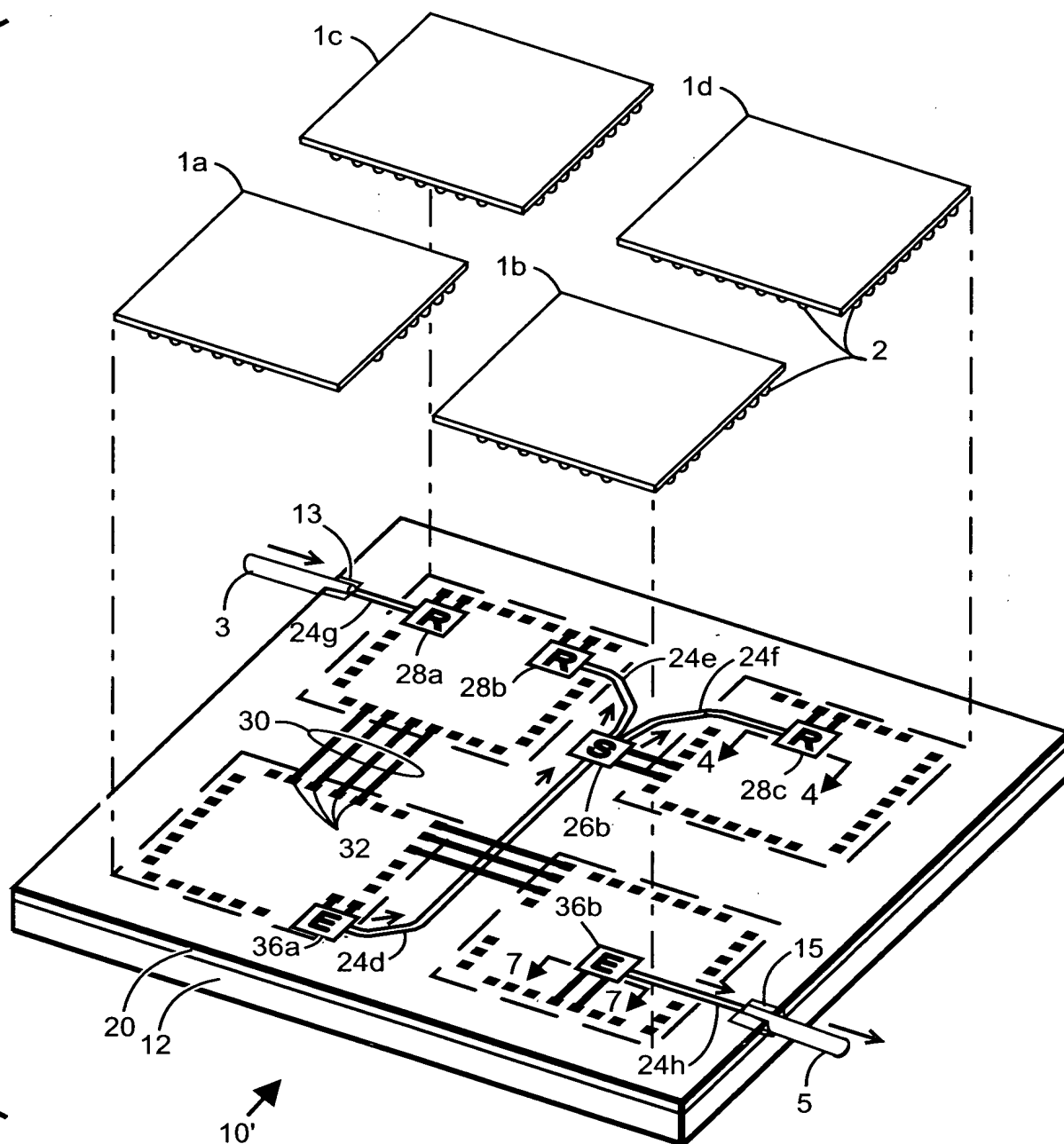


FIG. 6



6 / 61

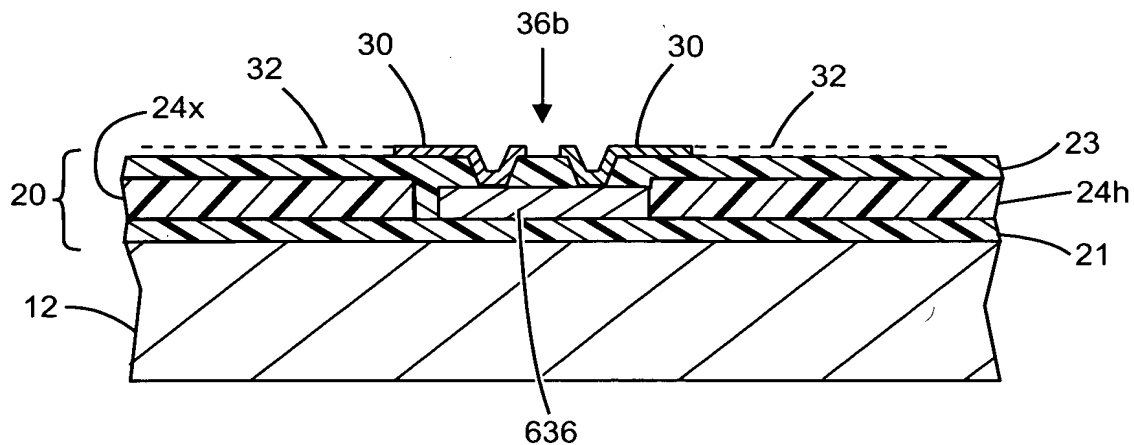


FIG._7

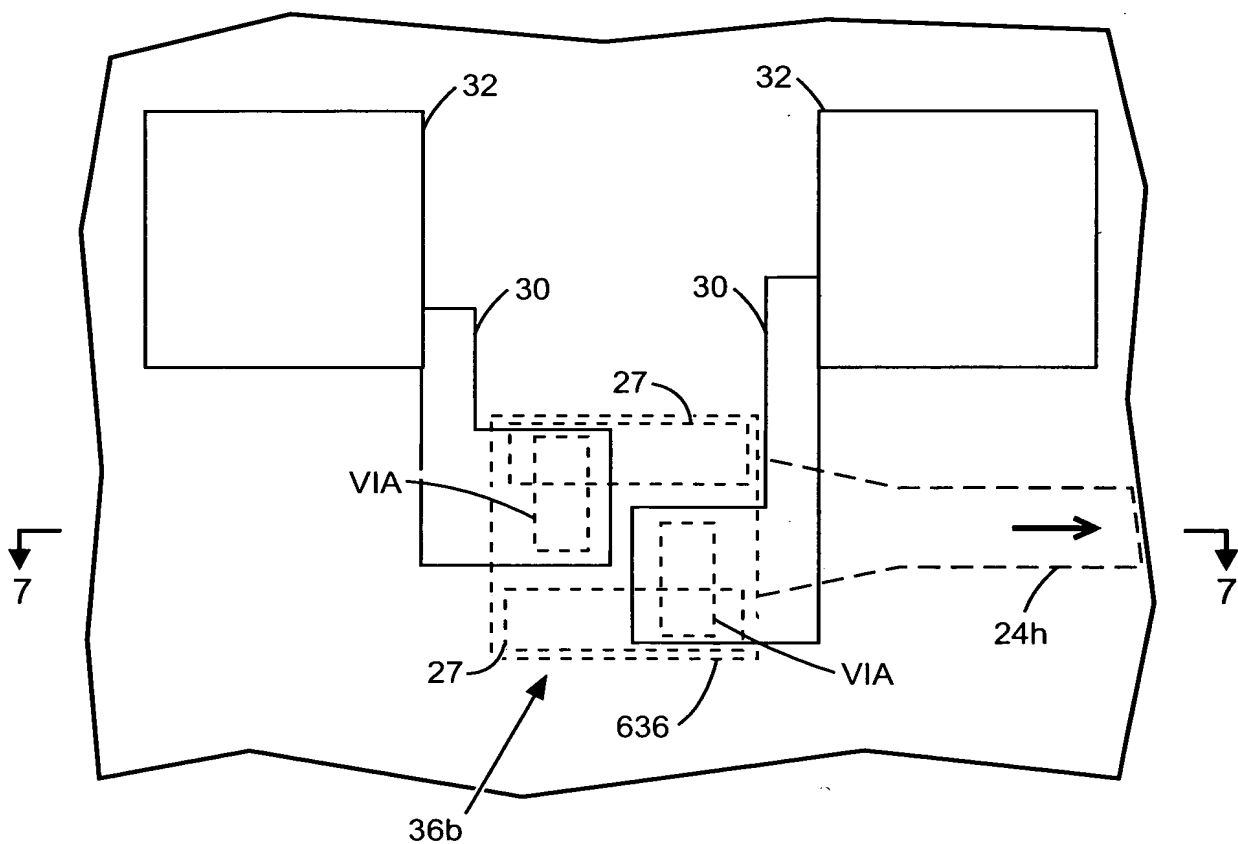


FIG._8





8 / 61

FIG._11

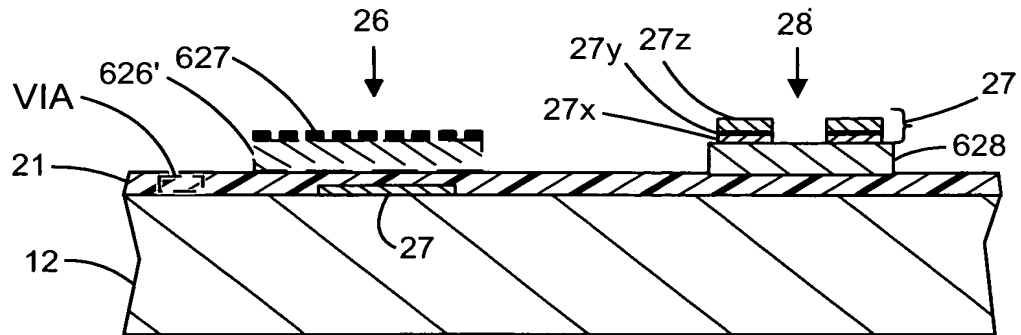


FIG._12

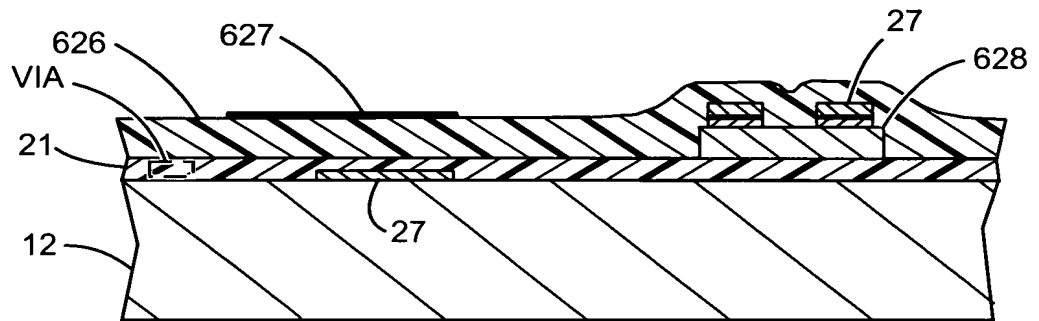


FIG._13

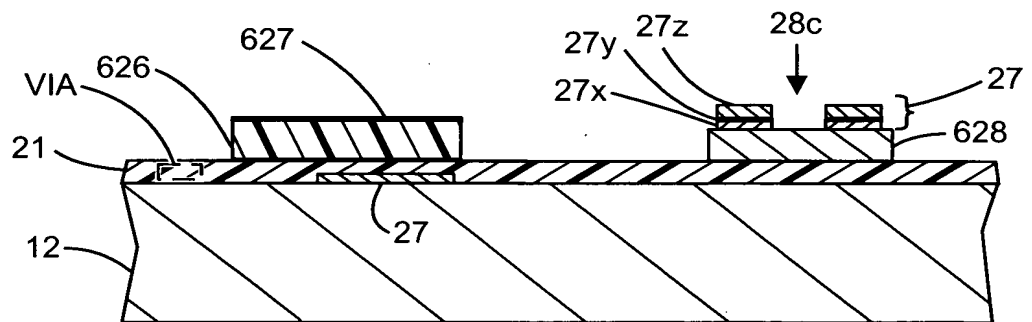
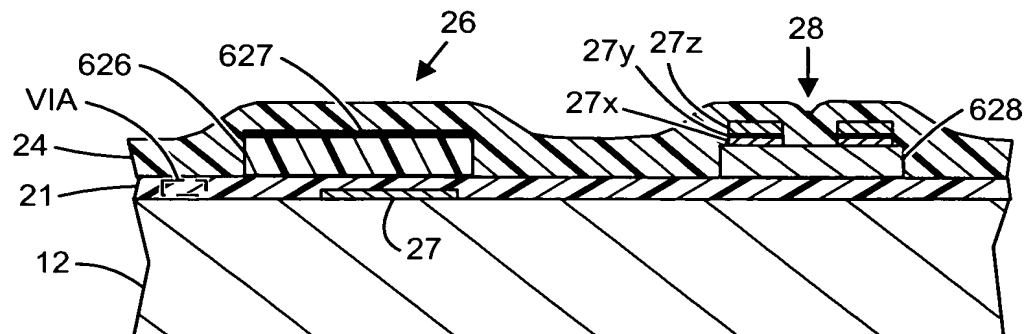
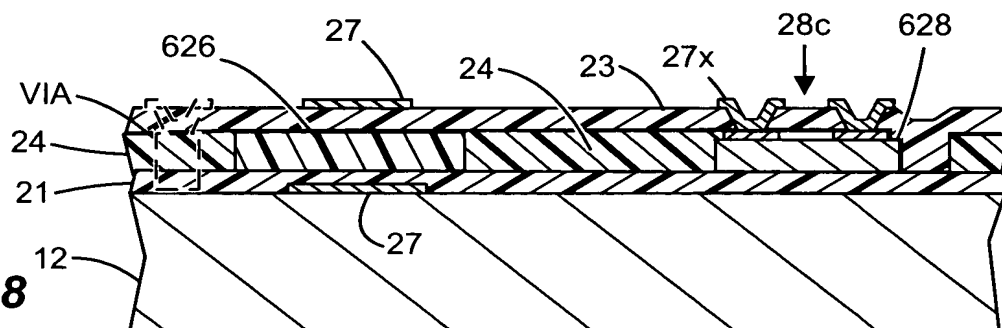
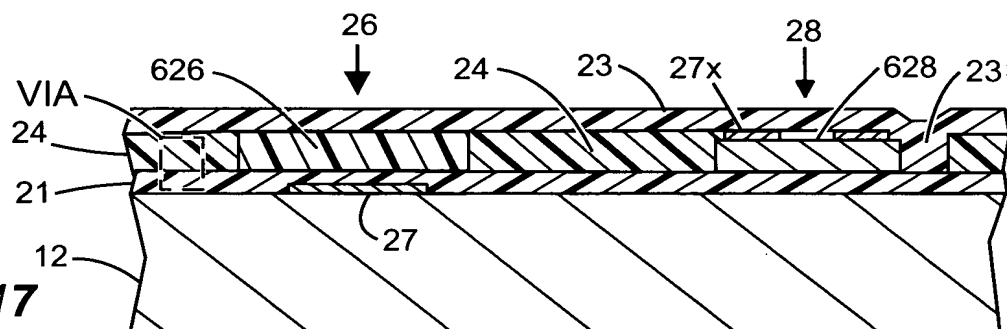
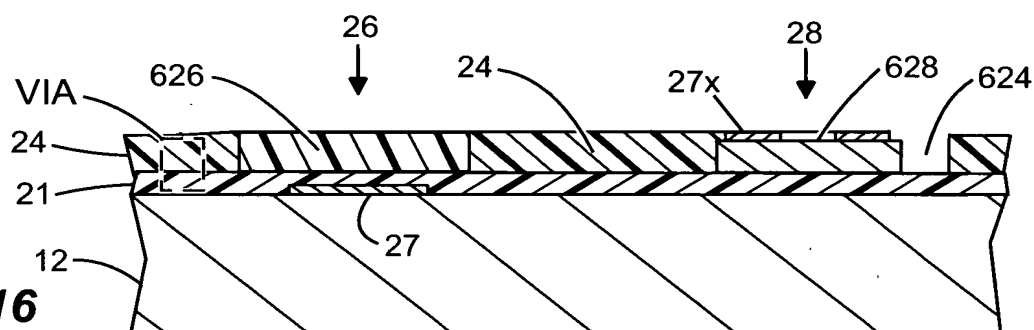
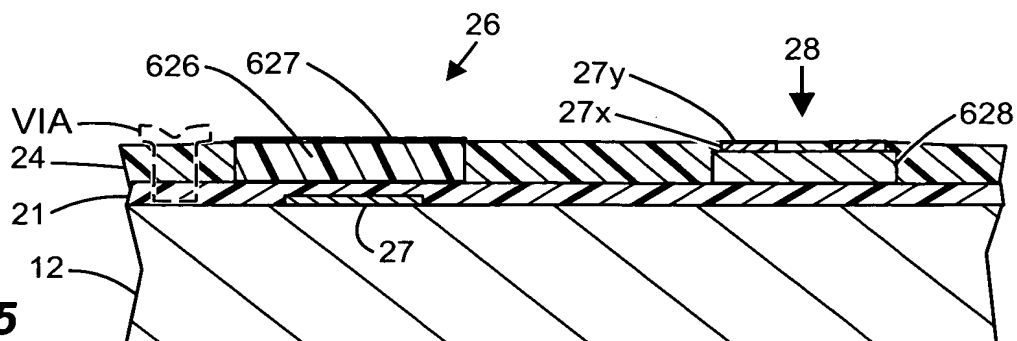


FIG._14



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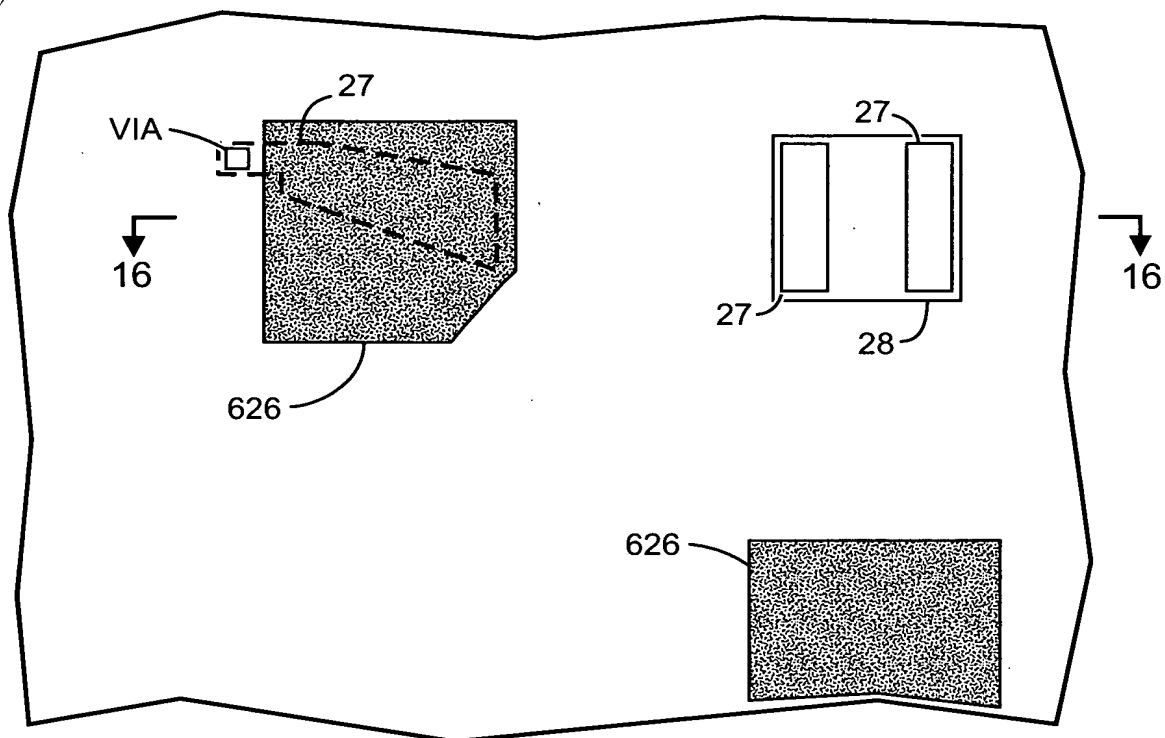


FIG. 19

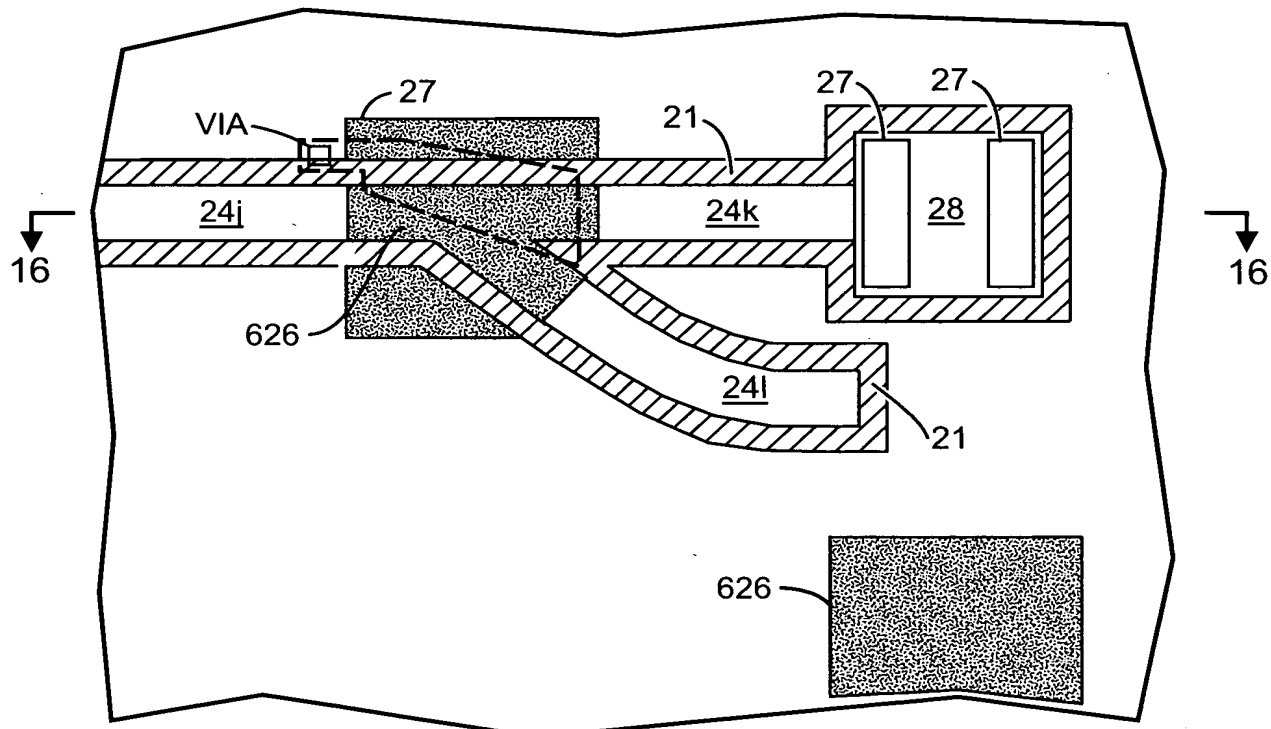


FIG. 20

Inventors: Tetsuzo Yoshimura, et al.
Application Serial No.: 09/295,431

11 / 61

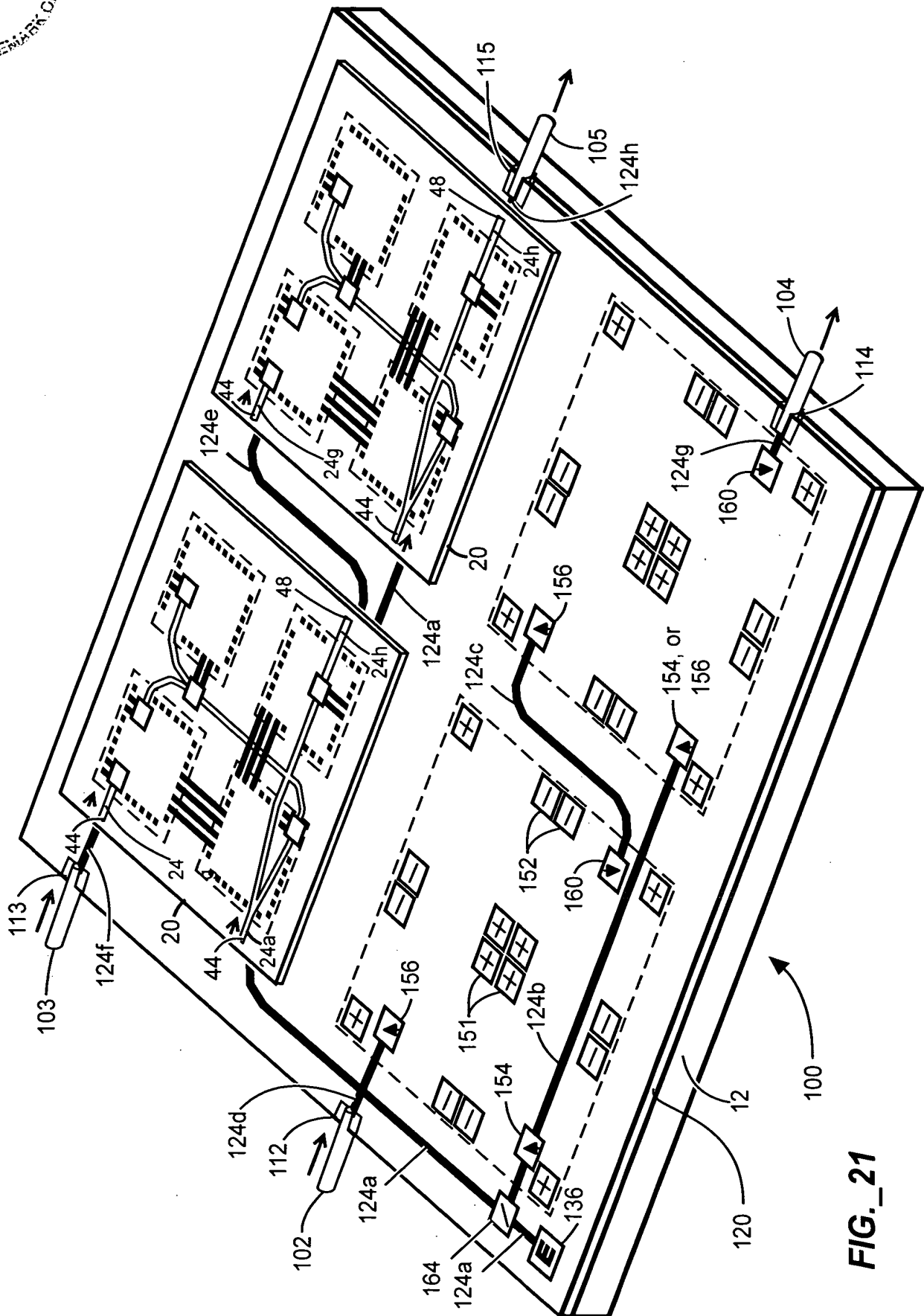


FIG. 21

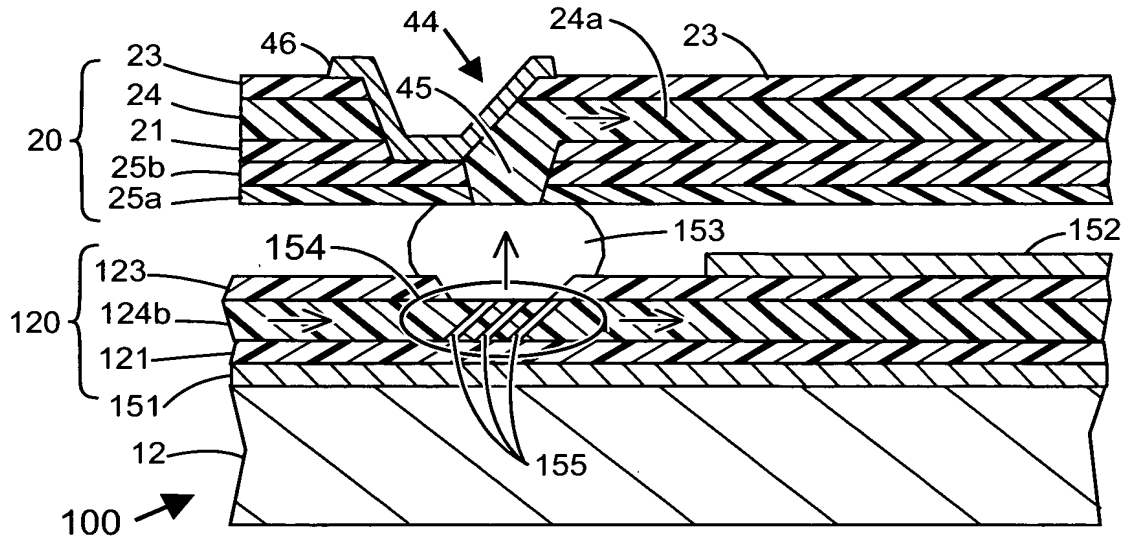


FIG._22

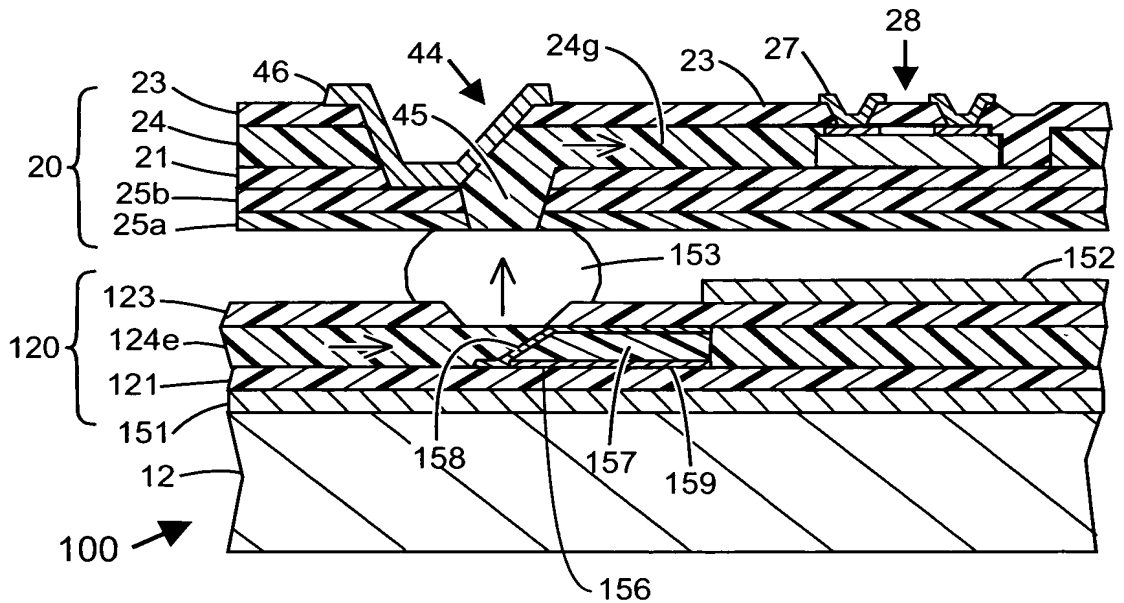


FIG._23

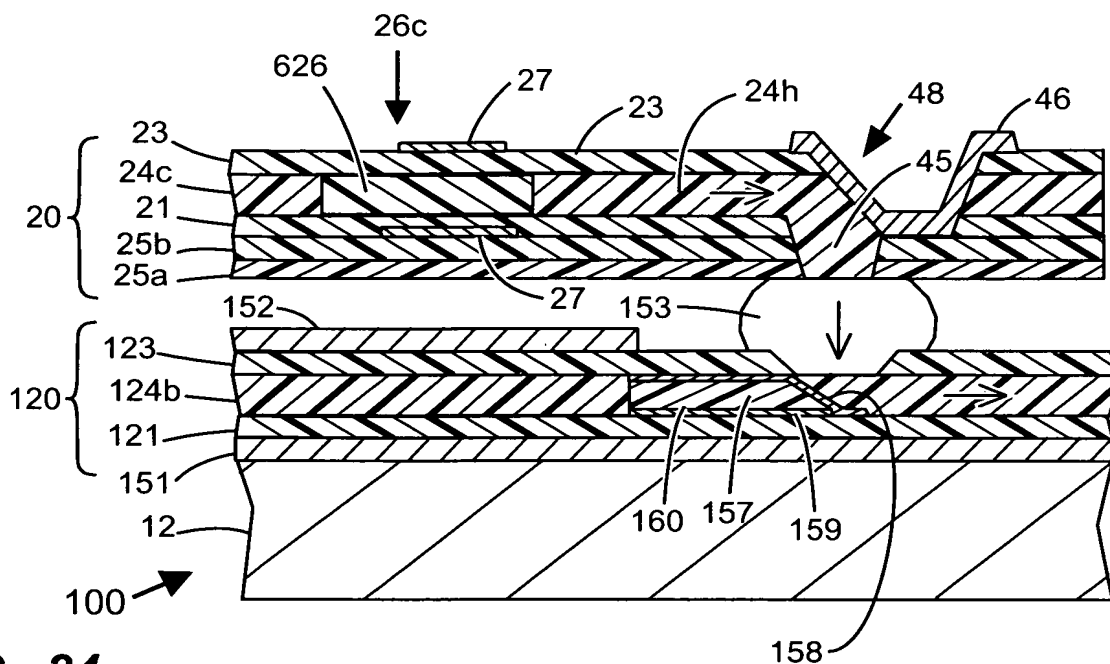


FIG. 24

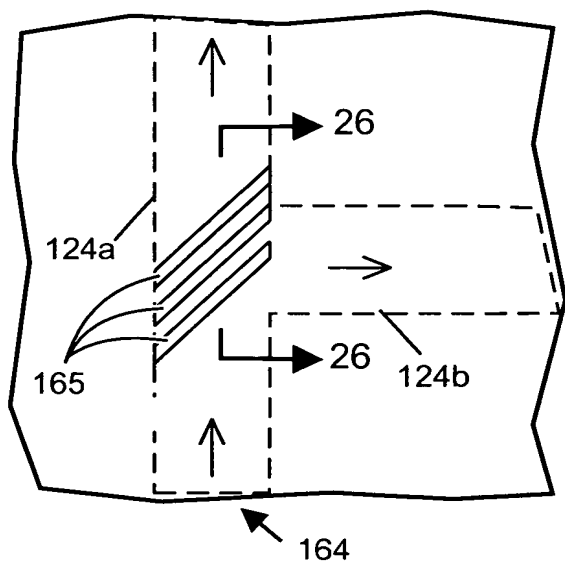


FIG. 25

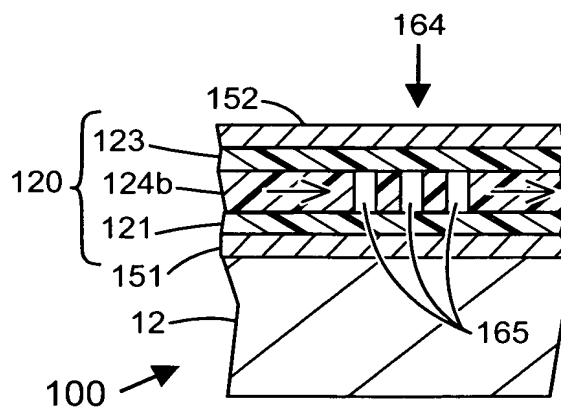
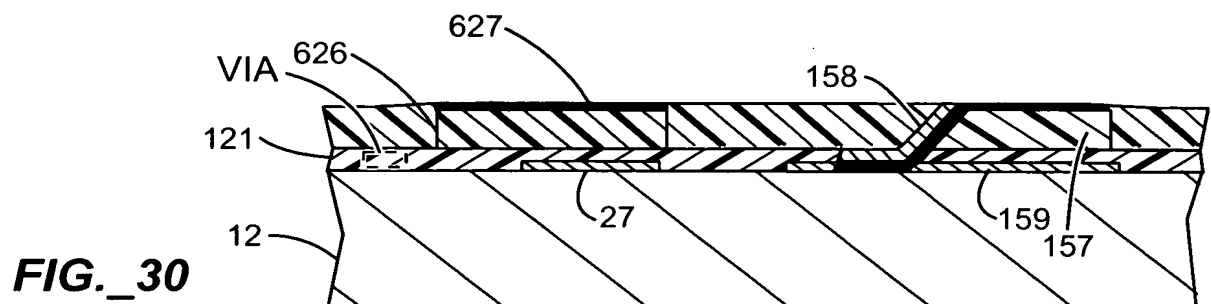
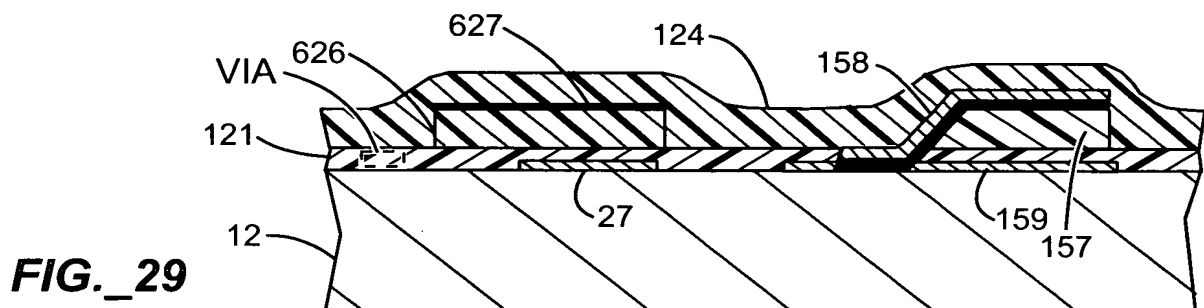
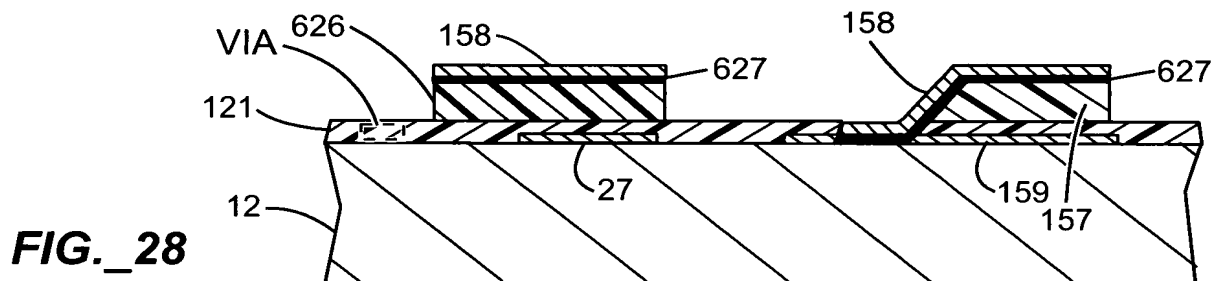
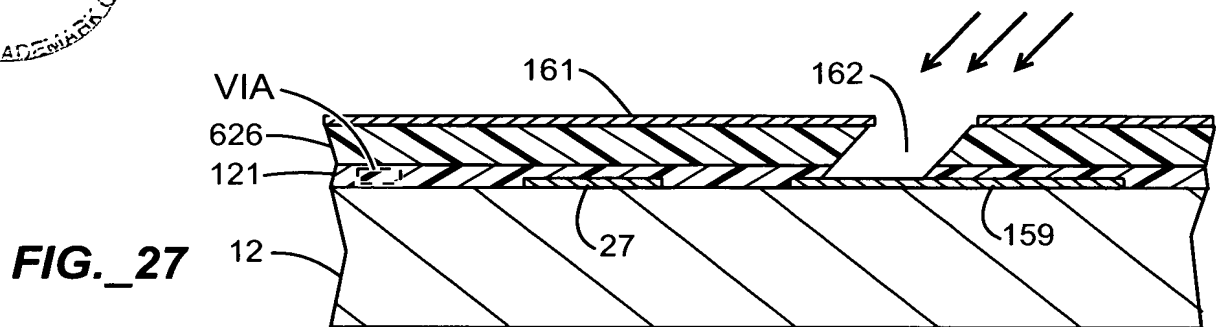


FIG. 26



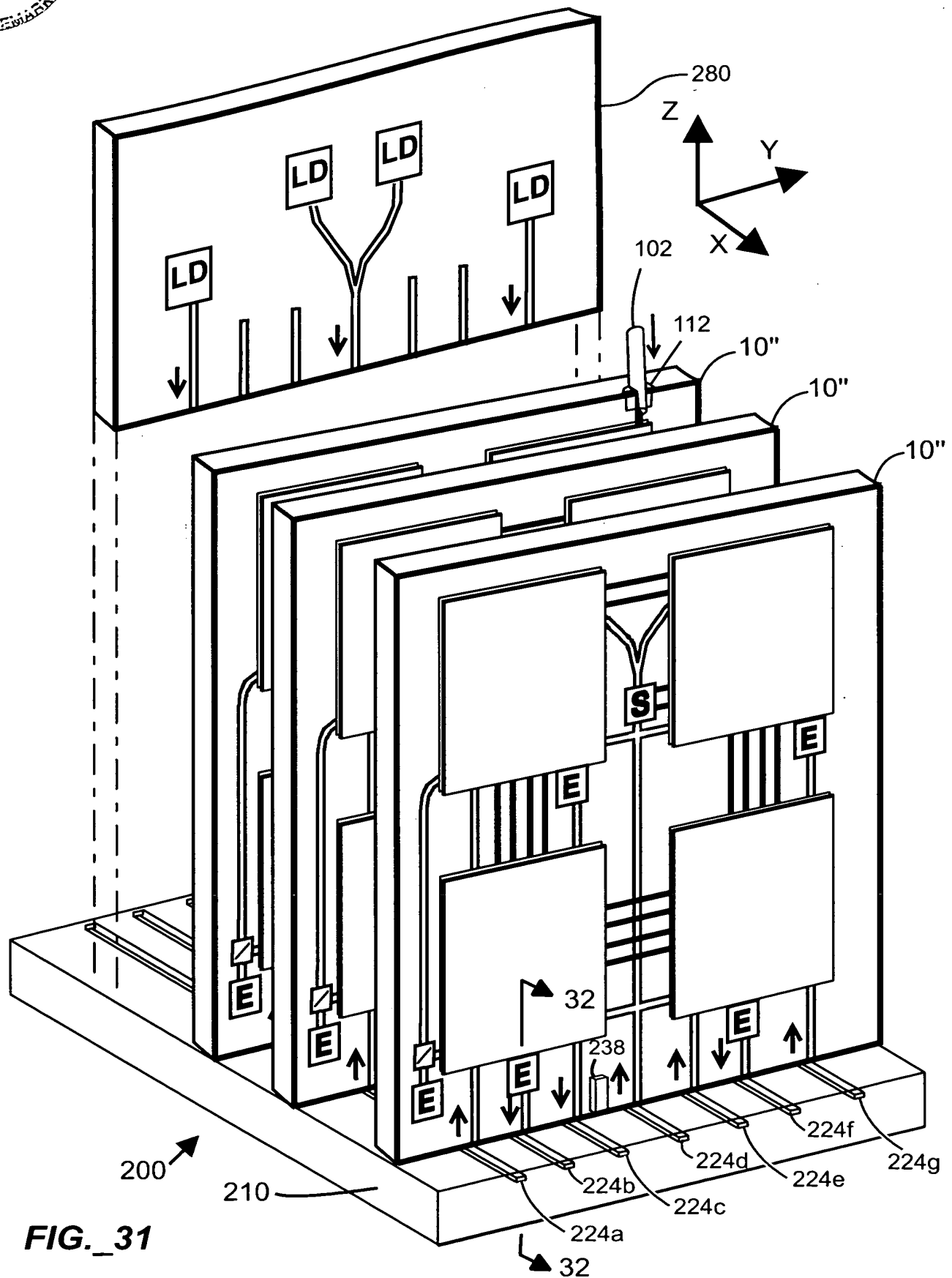


FIG. 31



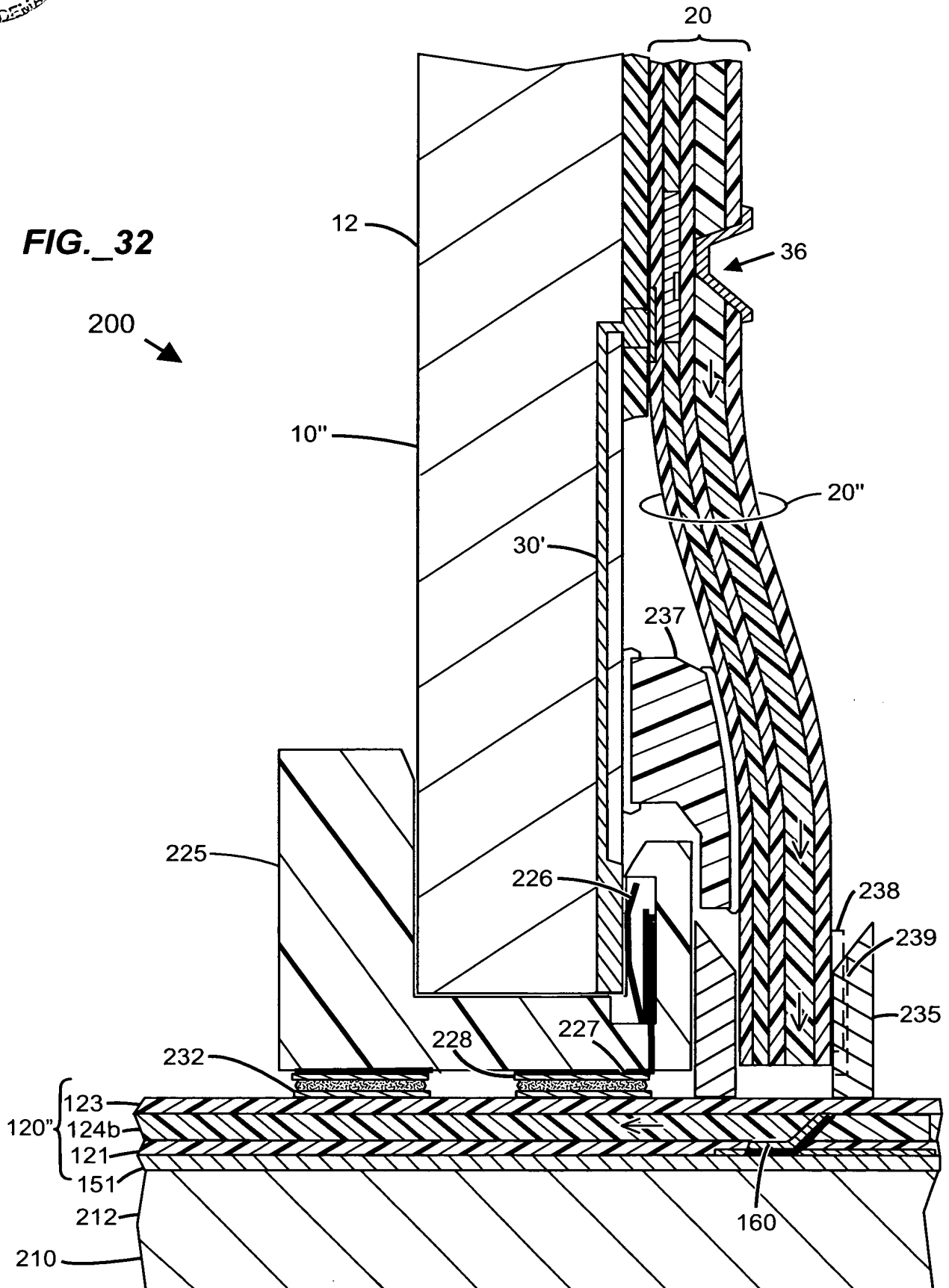
"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

16 / 61

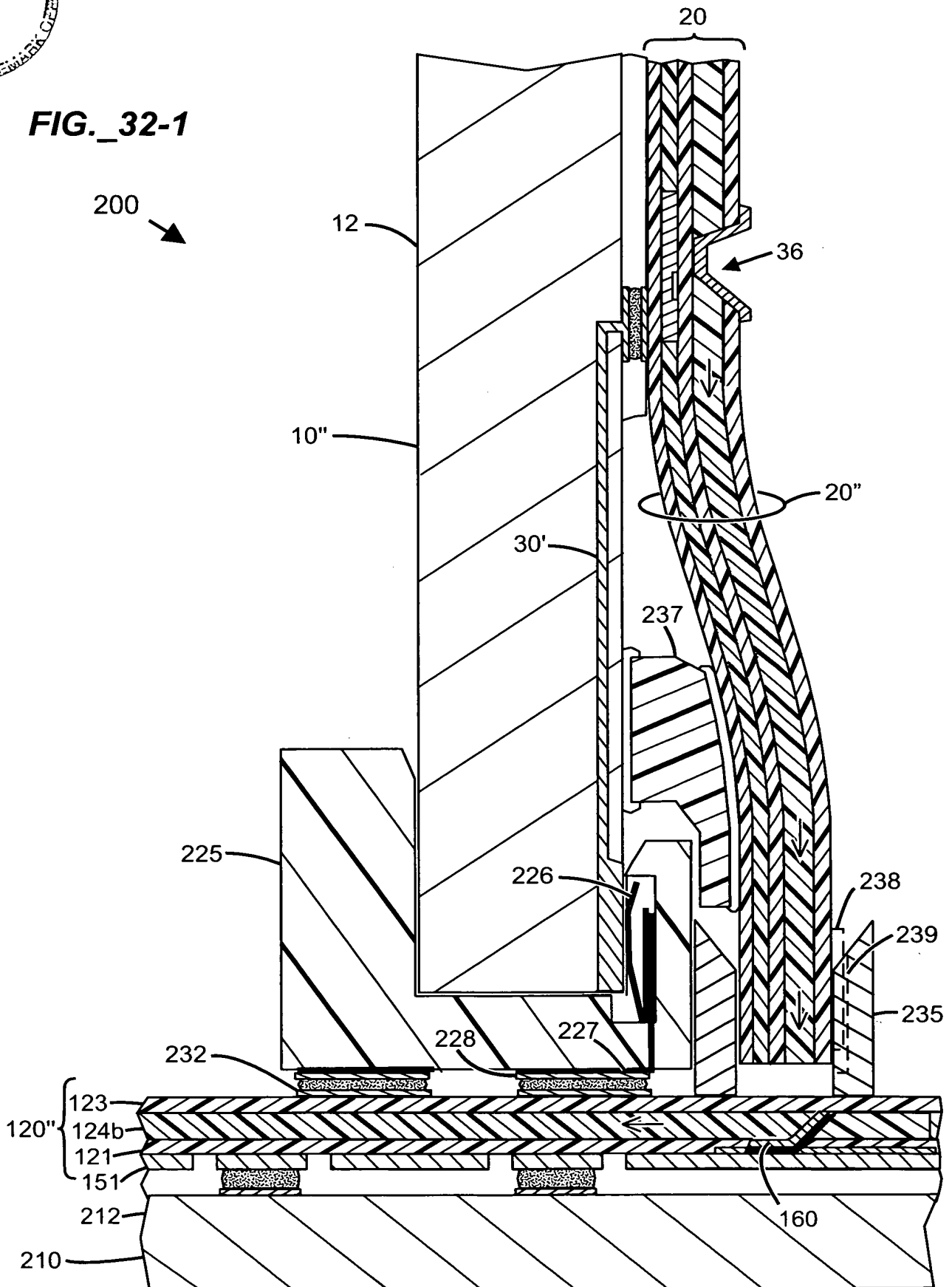
FIG. 32





17 / 61

FIG._32-1





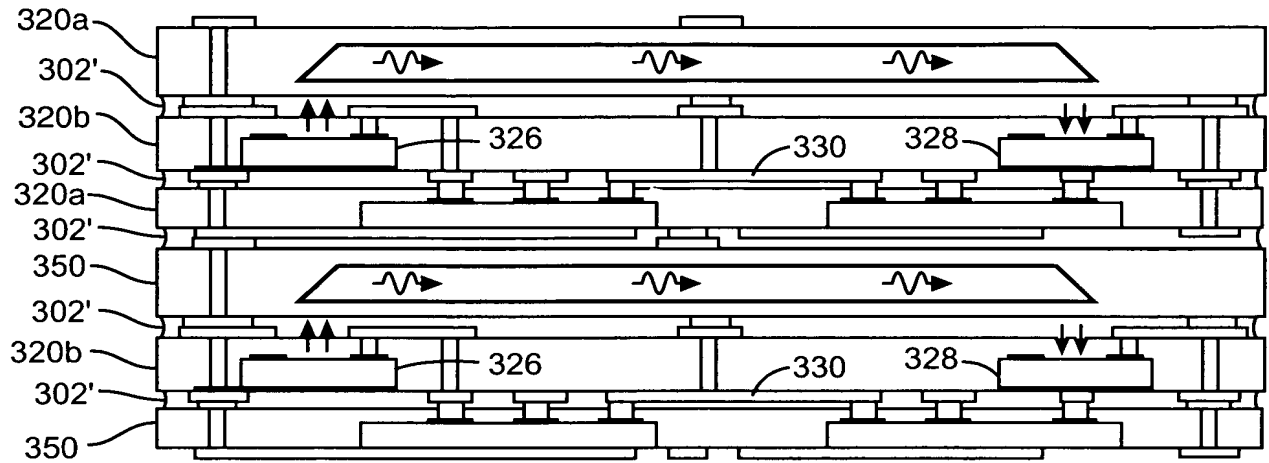


FIG. 36

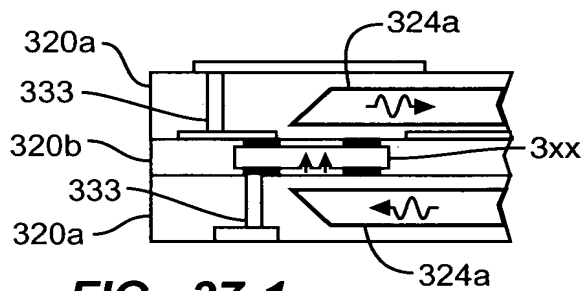


FIG. 37-1

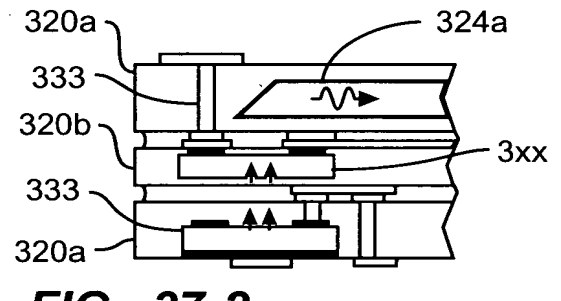


FIG. 37-2

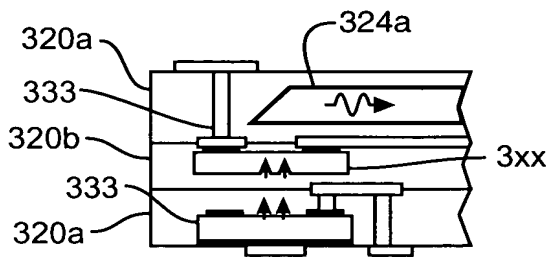


FIG. 37-3

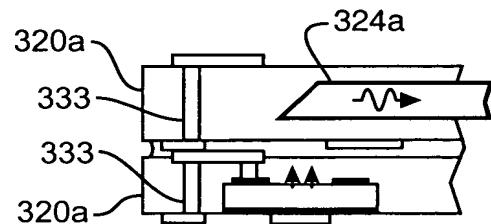


FIG. 37-4

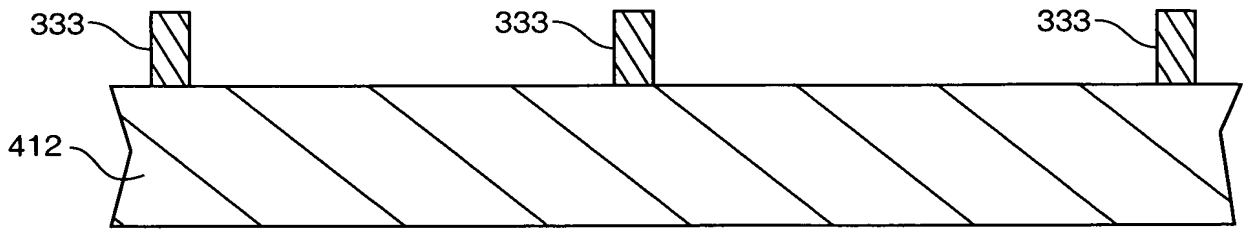


FIG._38

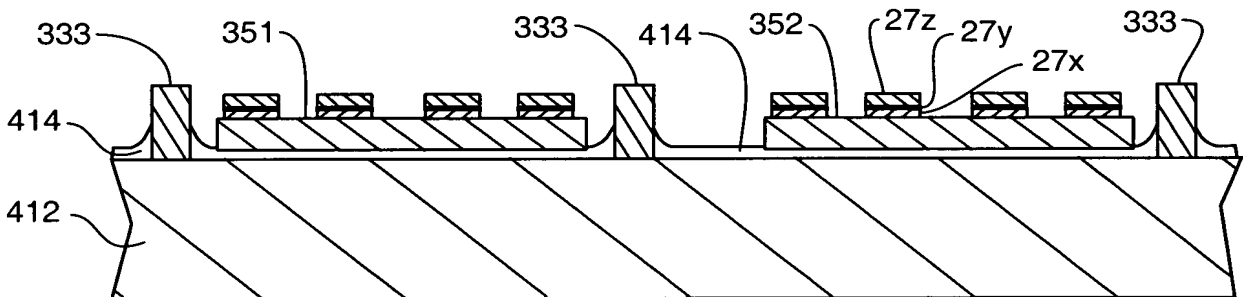


FIG._39

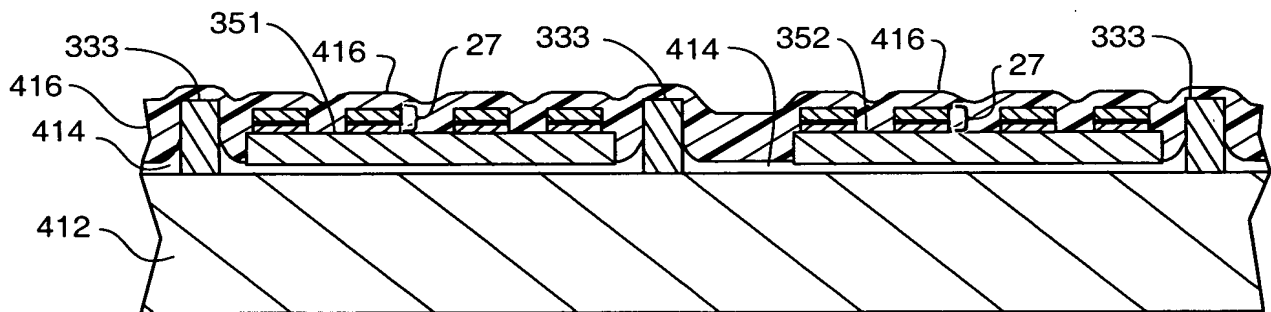


FIG._40

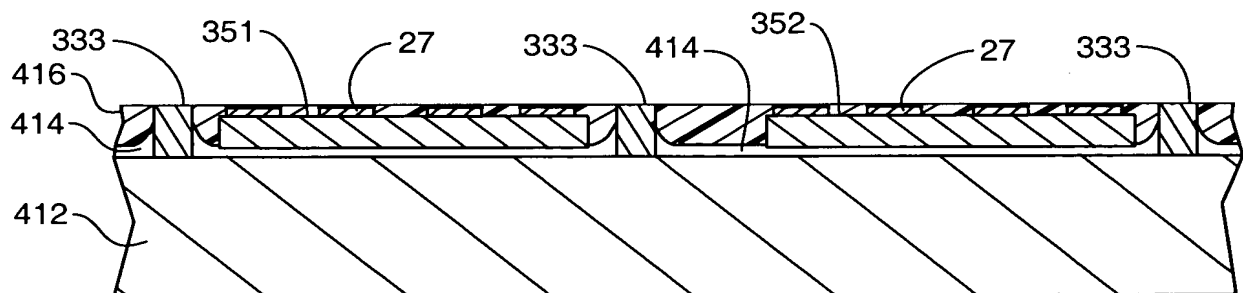


FIG._41

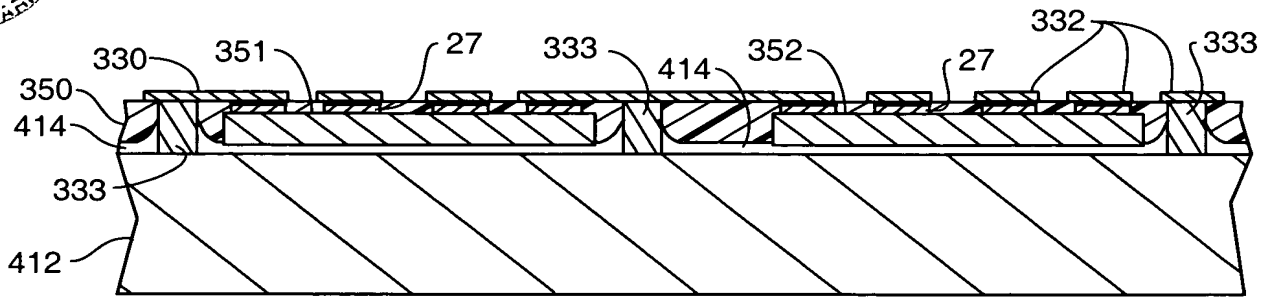


FIG. 42

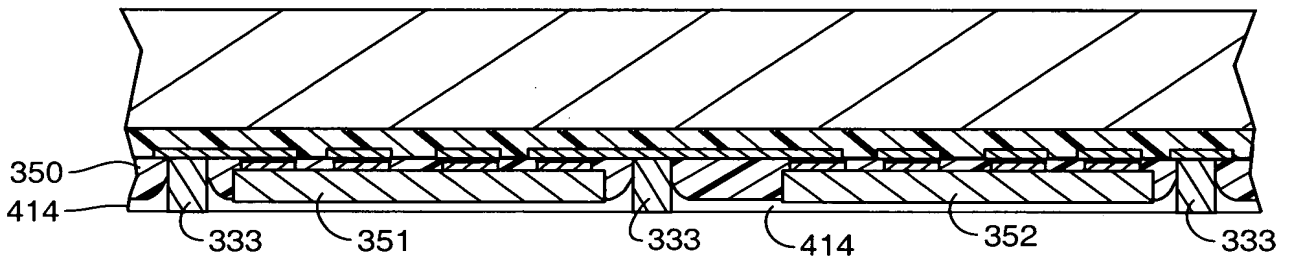


FIG. 43

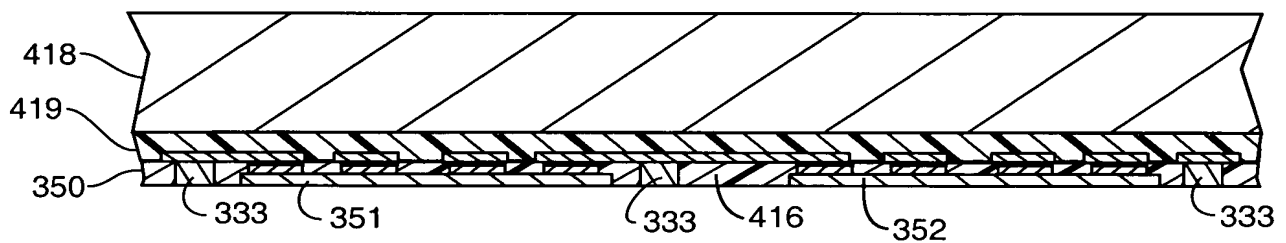


FIG. 44

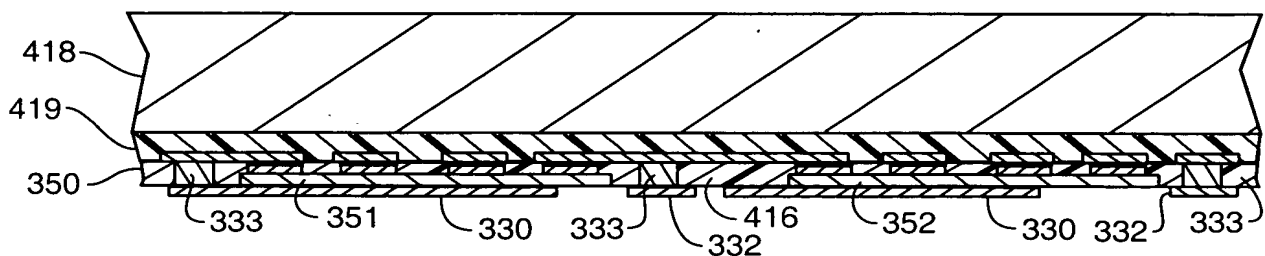
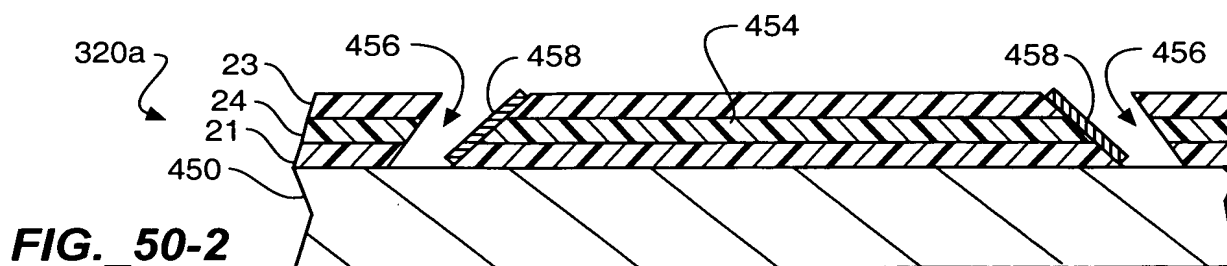
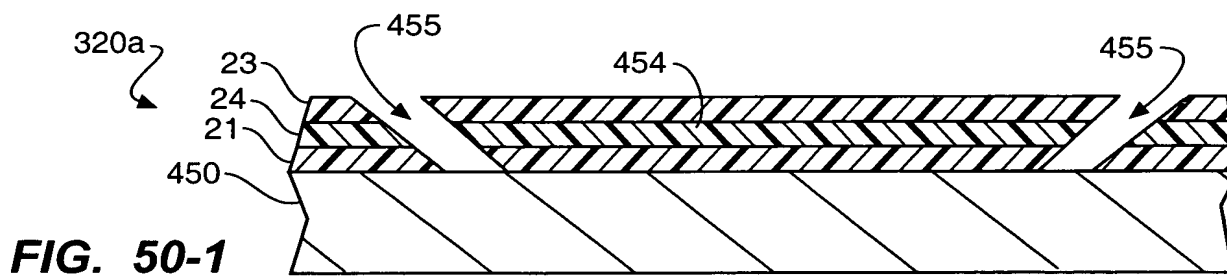
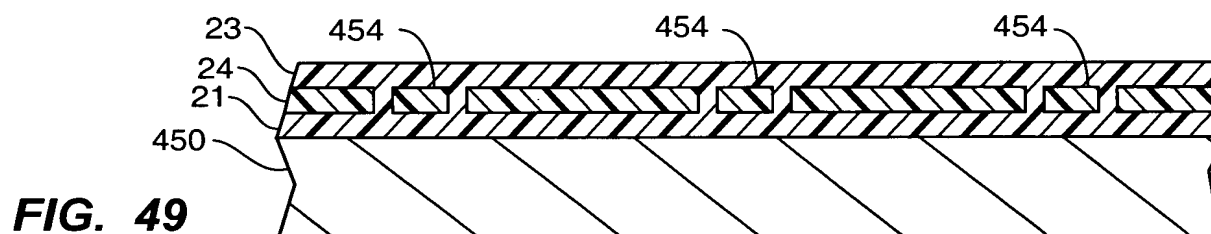
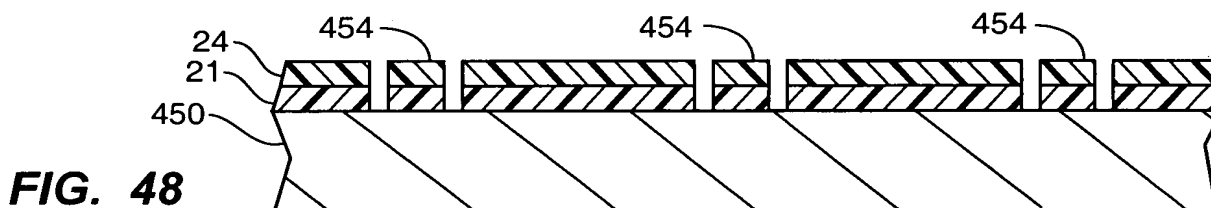
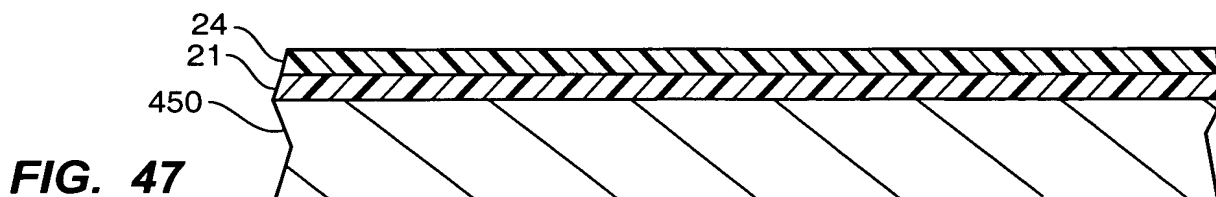
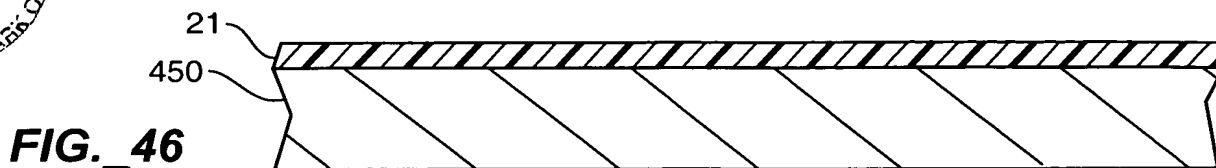


FIG. 45



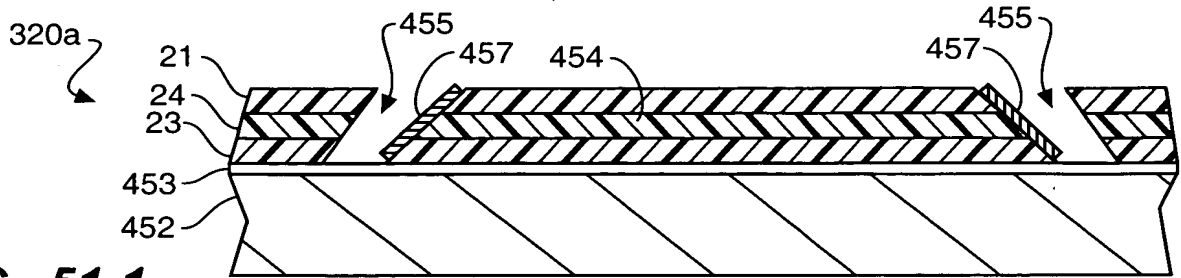


FIG. 51-1

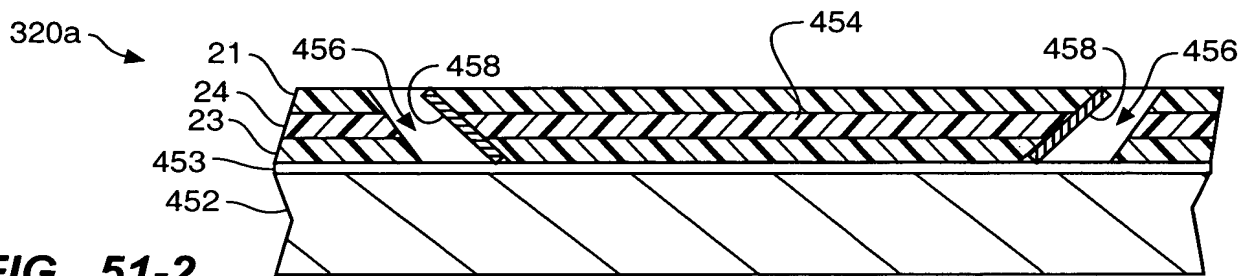


FIG. 51-2

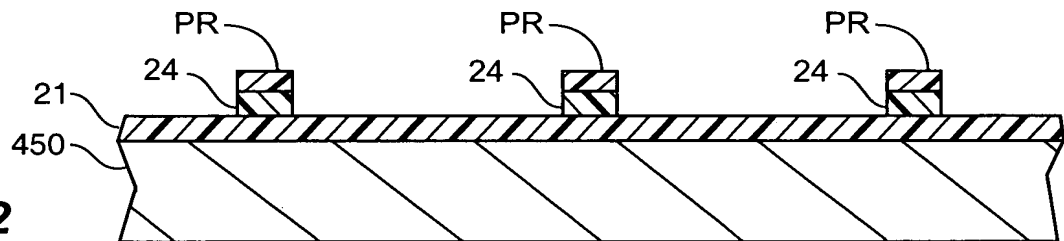


FIG. 52

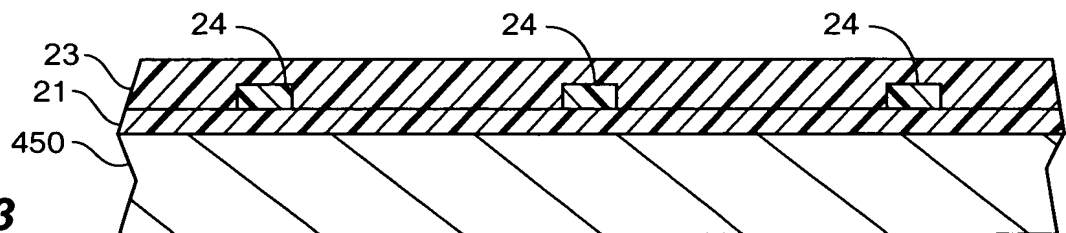
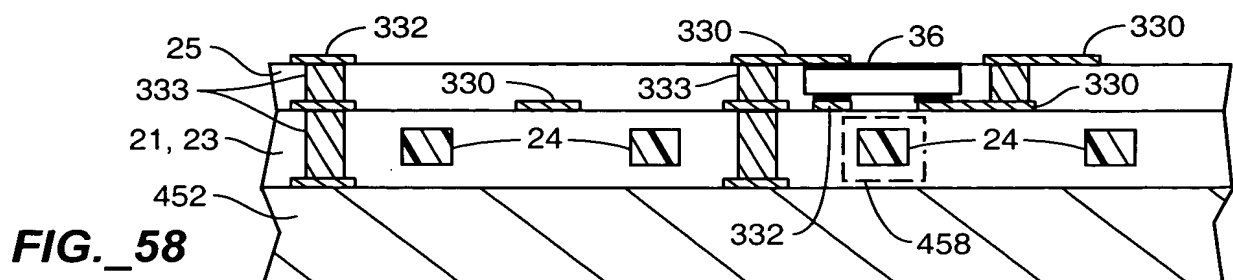
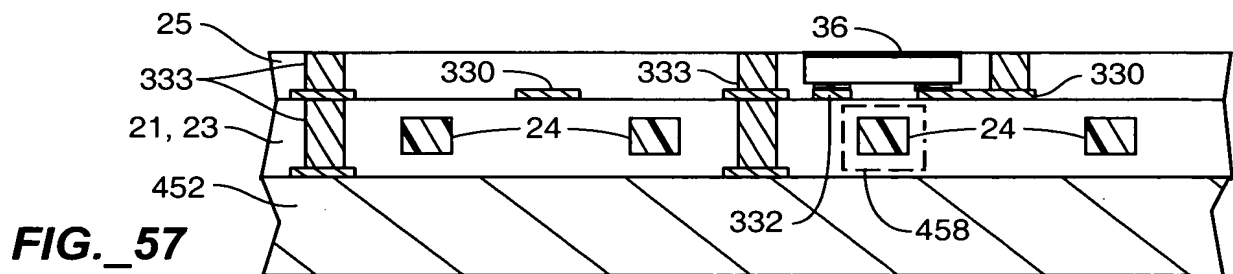
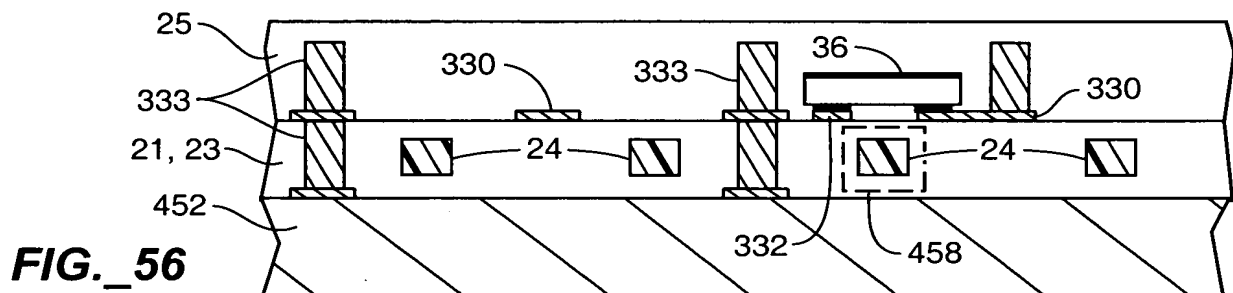
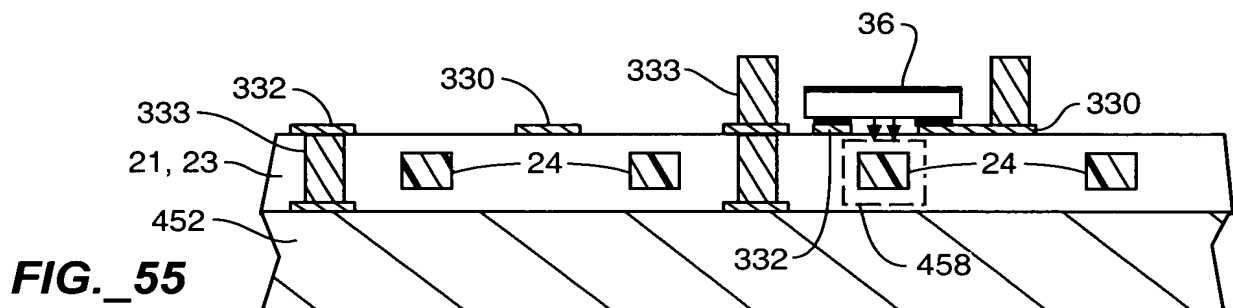
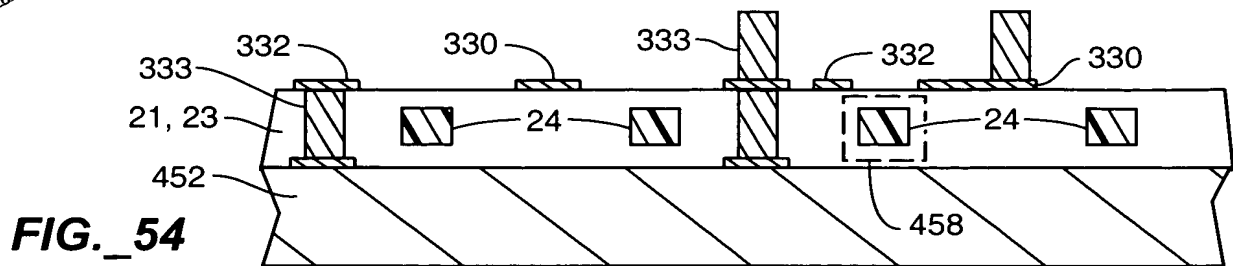
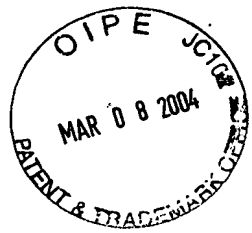


FIG. 53



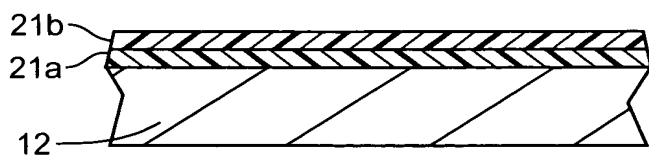


FIG. 59

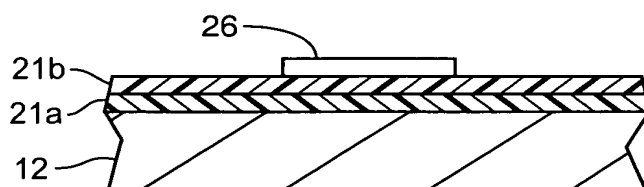


FIG. 60

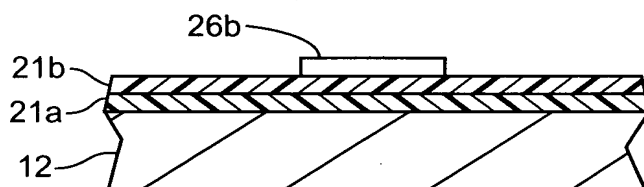


FIG. 62

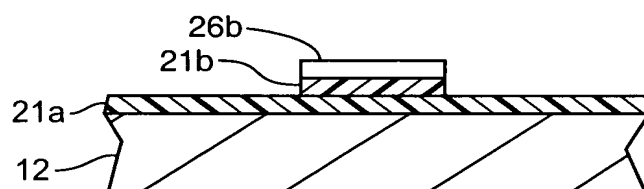


FIG. 64

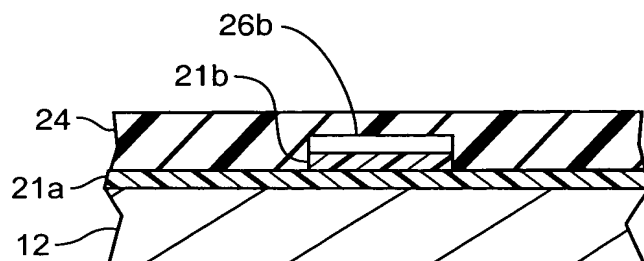


FIG. 65

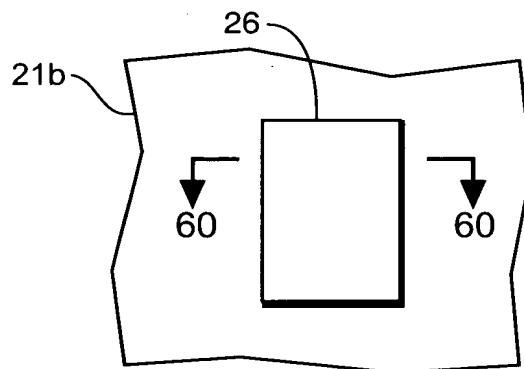


FIG. 61

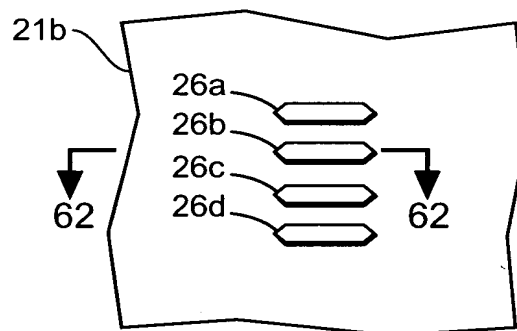


FIG. 63

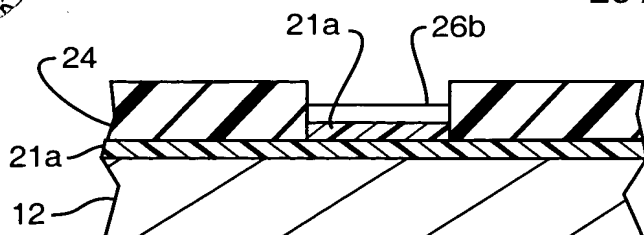


FIG. 66

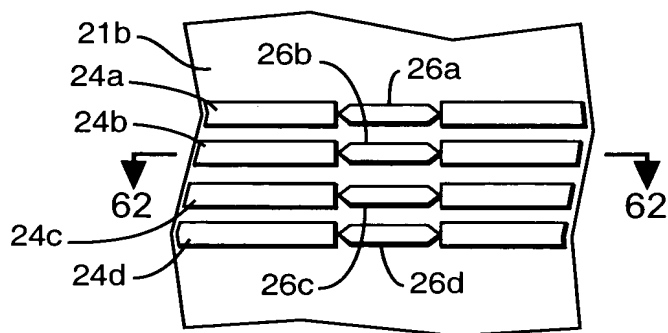


FIG. 67

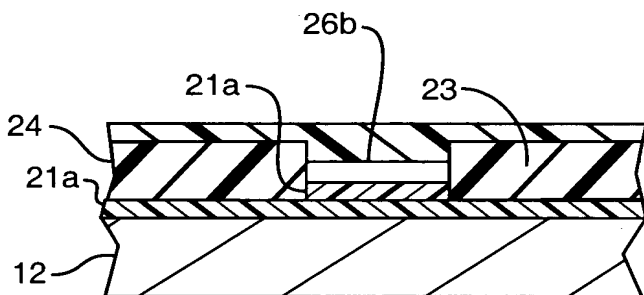


FIG. 68

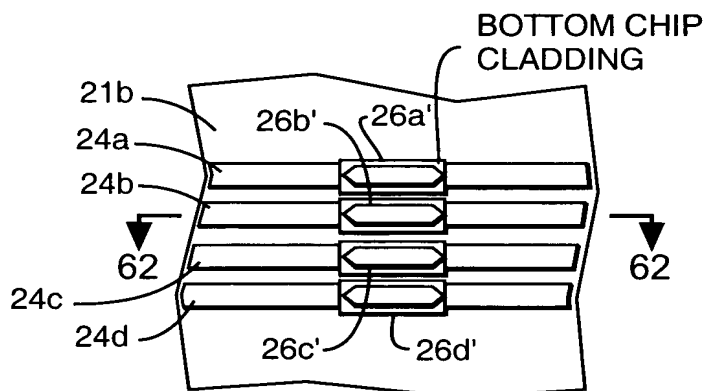


FIG. 67-2

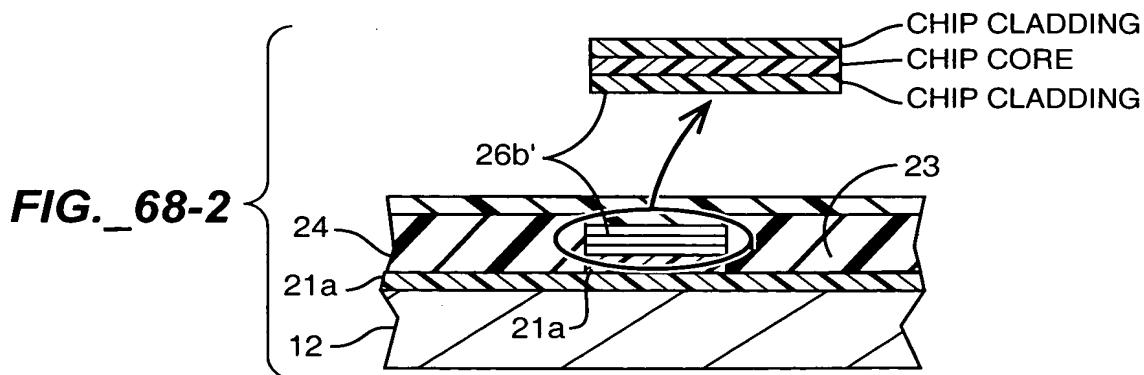


FIG. 68-2

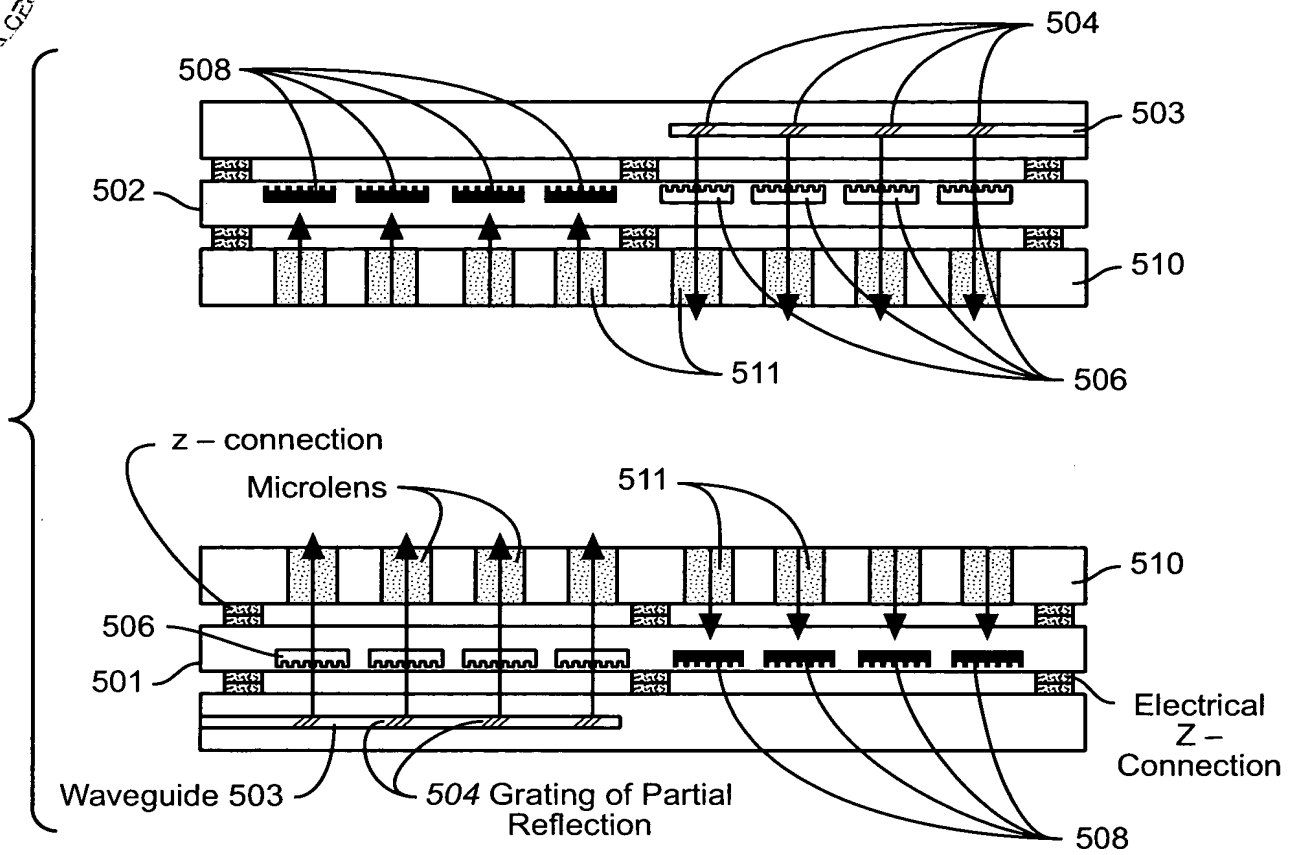
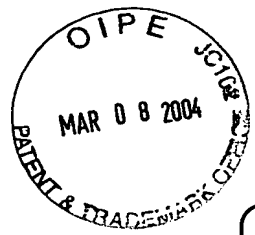


FIG. 69

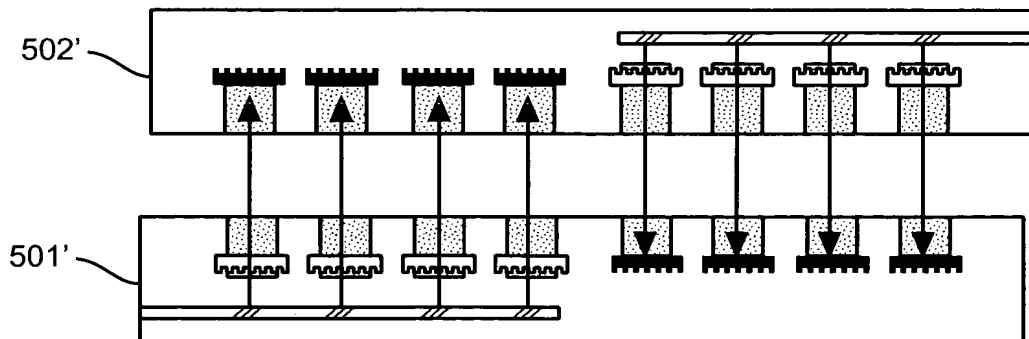


FIG. 70

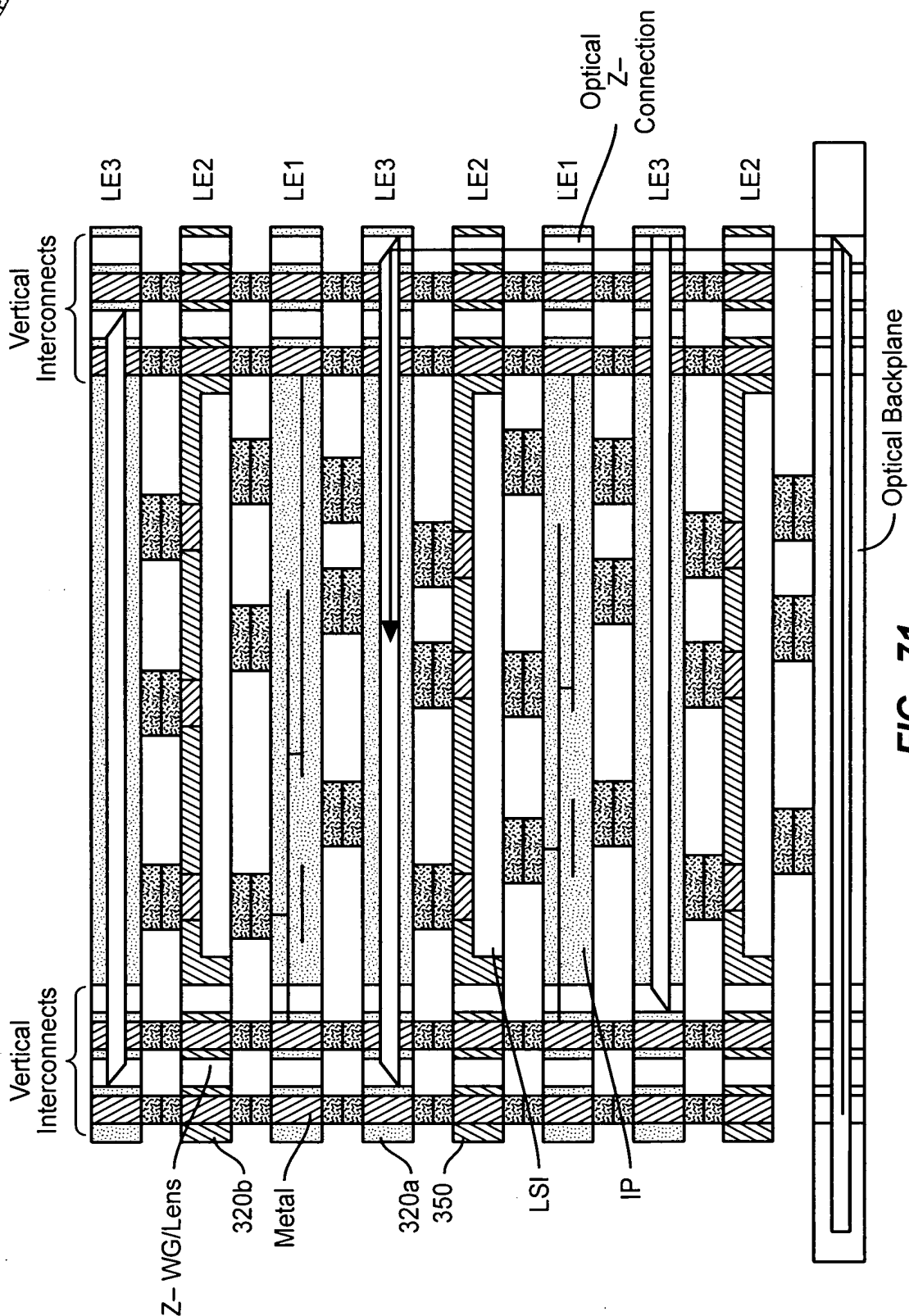
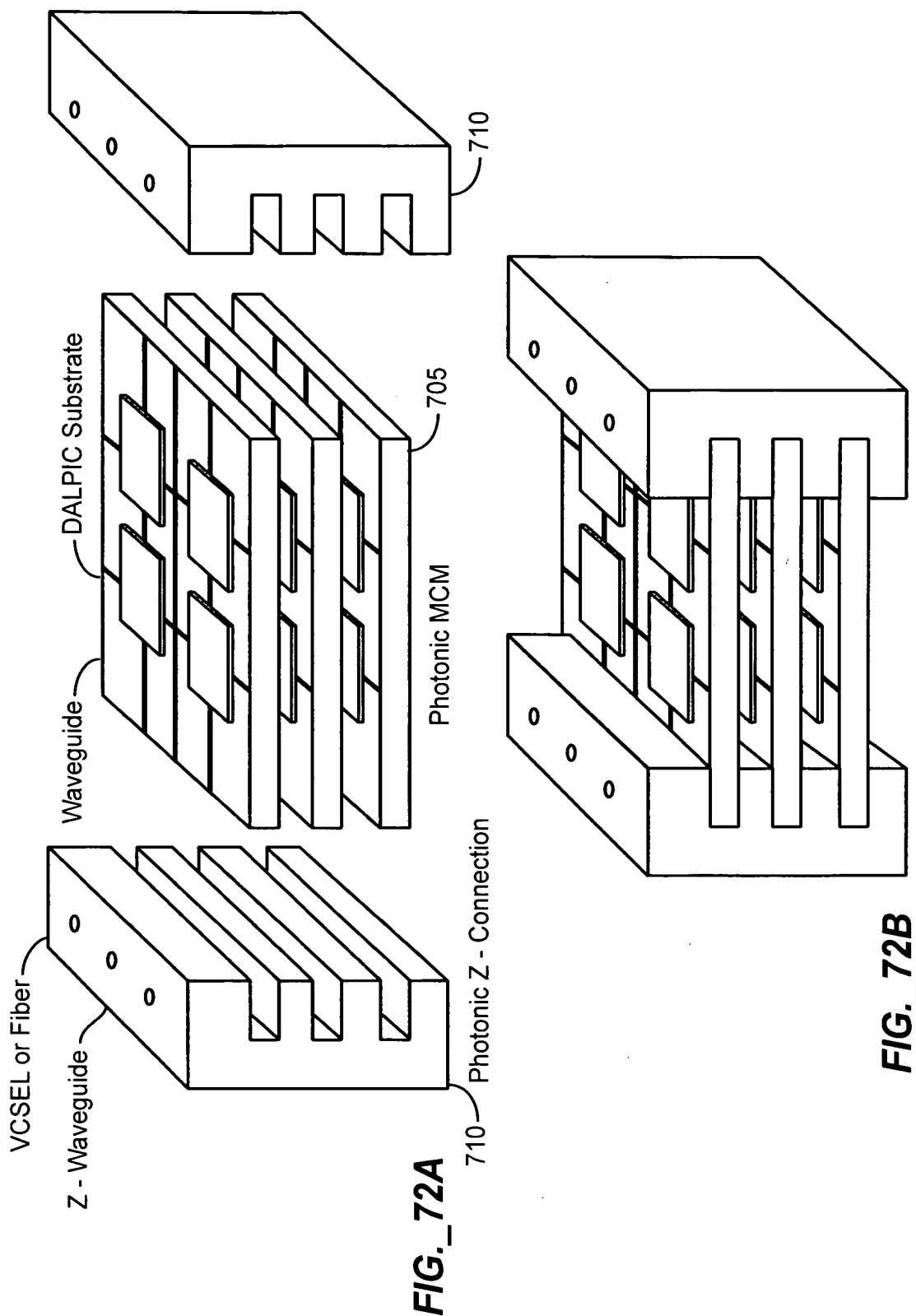


FIG. 71



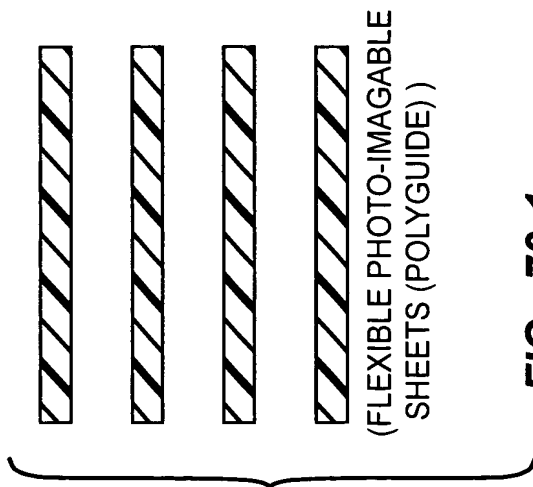


FIG. 73-1

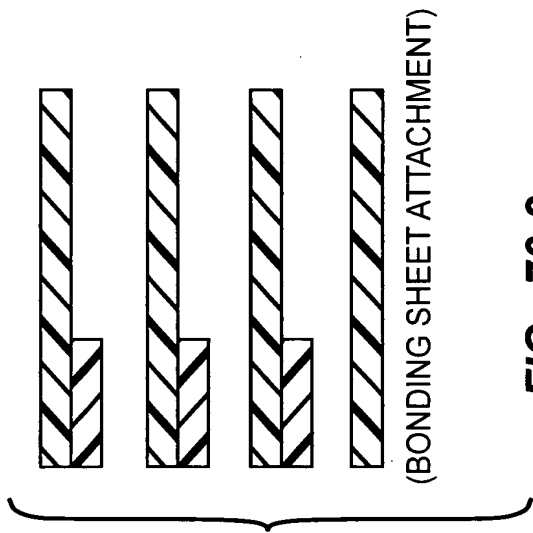


FIG. 73-2

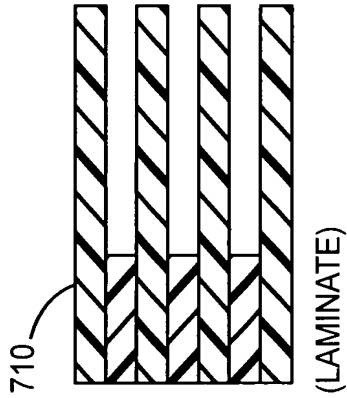


FIG. 73-3

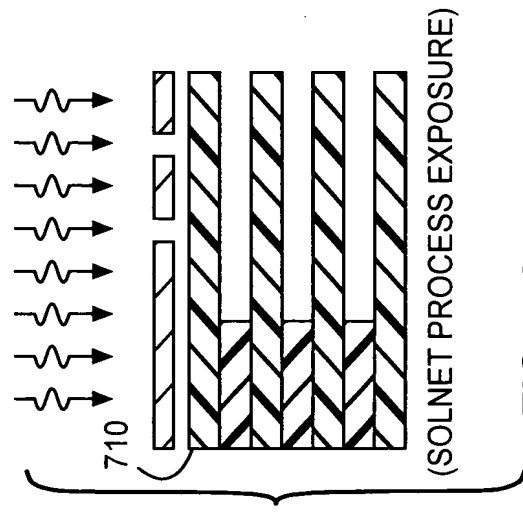


FIG. 73-4

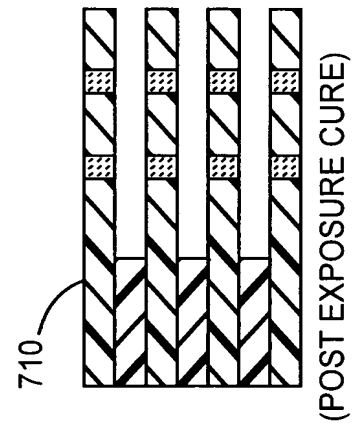


FIG. 73-5

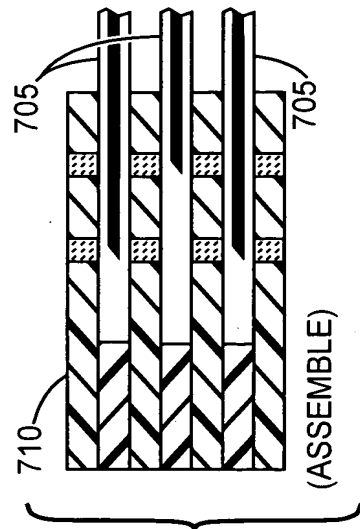
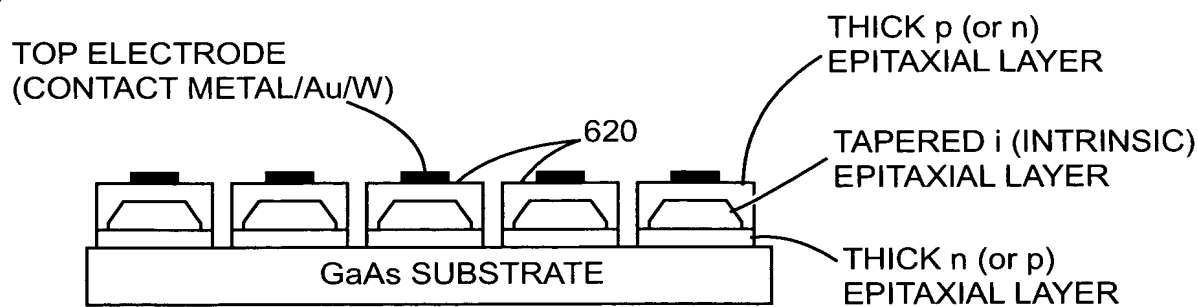
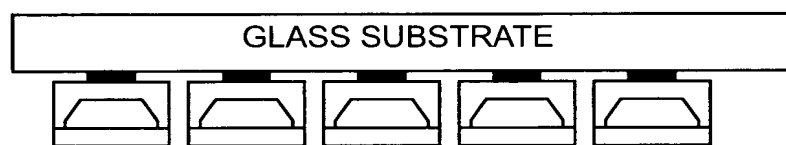


FIG. 73-6



(EPITAXIAL GROWTH AND PATTERNING)

FIG._74



(EPITAXIAL LIFTOFF)

FIG._75

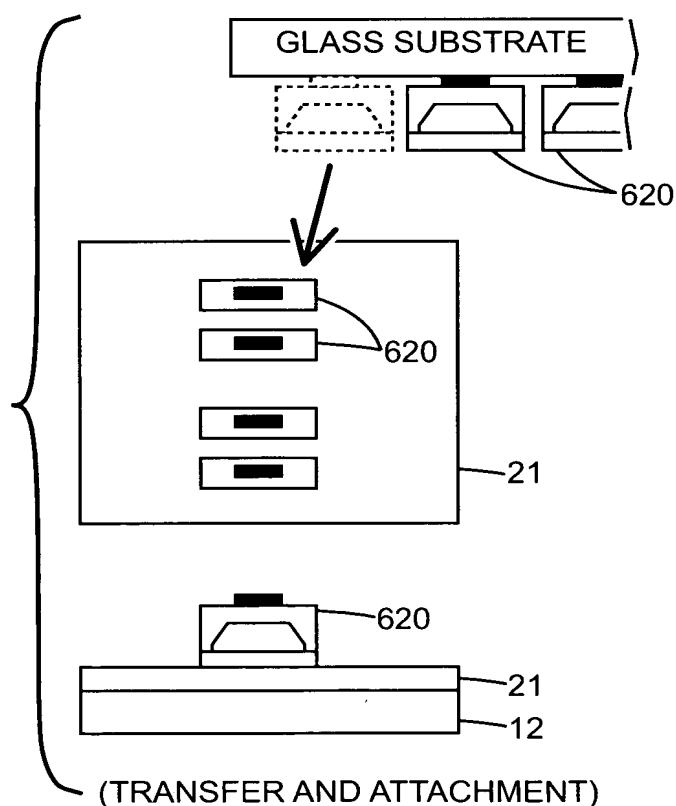


FIG._76

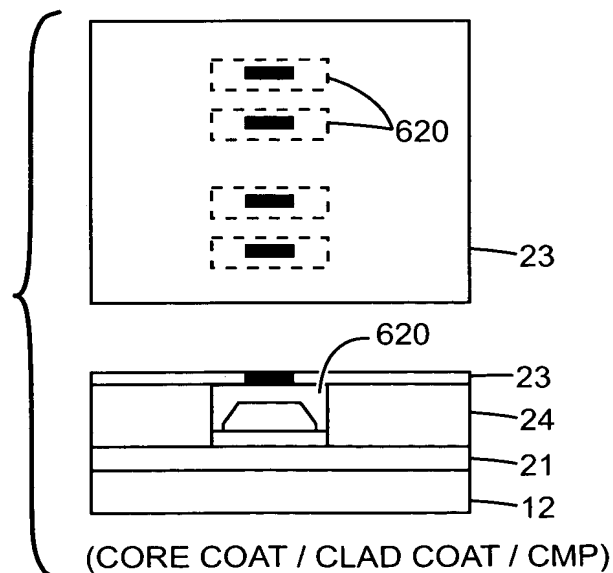


FIG._77

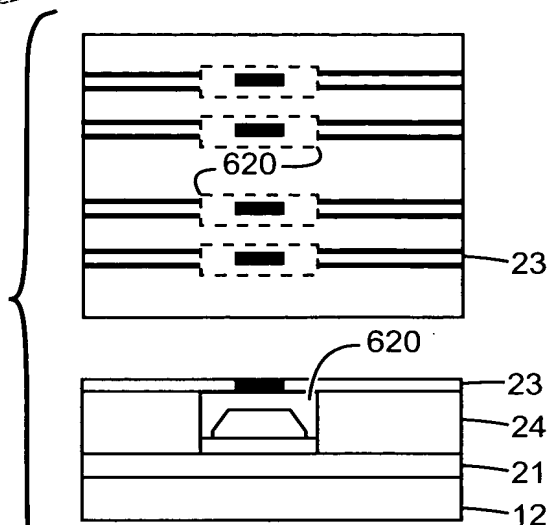


FIG. 78 (CORE PATTERNING)

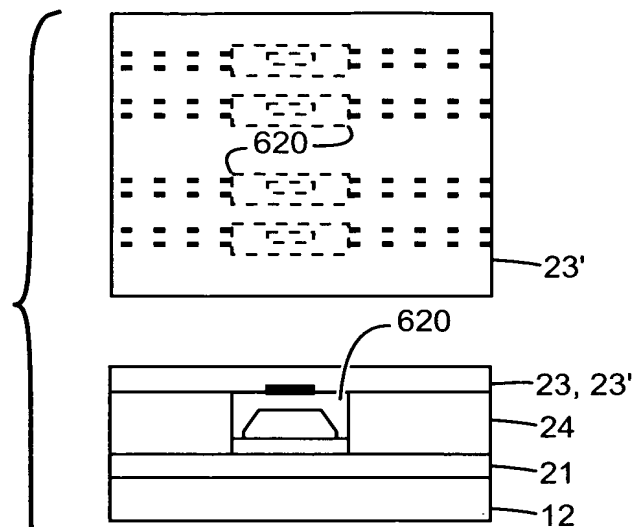
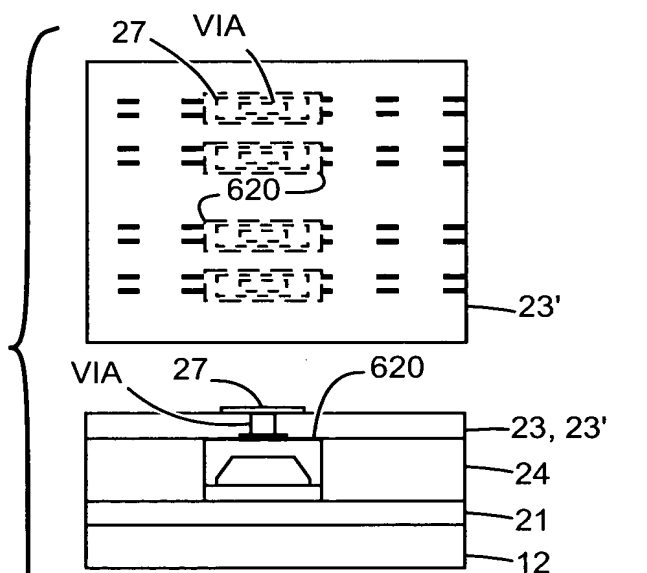
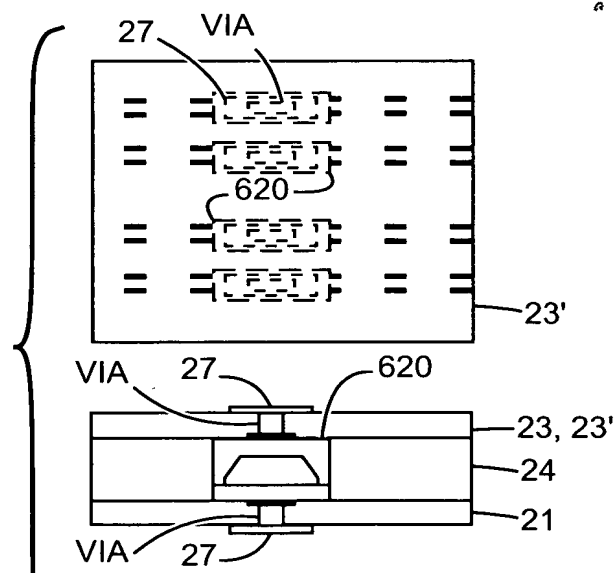


FIG. 79 (CLAD COATING)



(VIA AND ELECTRODE FORMATION)

FIG. 80



(SUBSTRATE REMOVAL /
BACK-SIDE METALIZATION)

FIG. 81



TOP ELECTRODE
(CONTACT METAL/Au/W)

THICK p (or n)
EPITAXIAL LAYER

TAPERED i (INTRINSIC)
EPITAXIAL LAYER (~CORE)

THICK n (or p)
EPITAXIAL LAYER

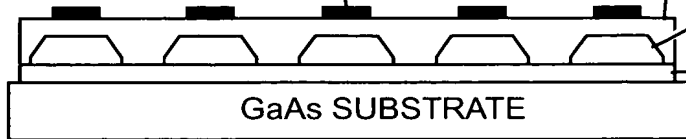


FIG. 82

(EPITAXIAL GROWTH)

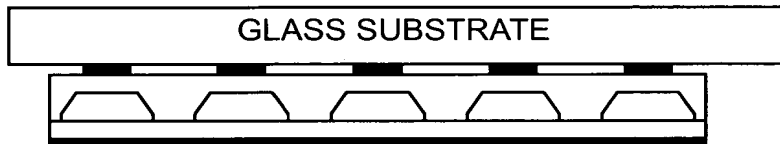


FIG. 83

(EPITAXIAL LIFTOFF AND METALIZATION)

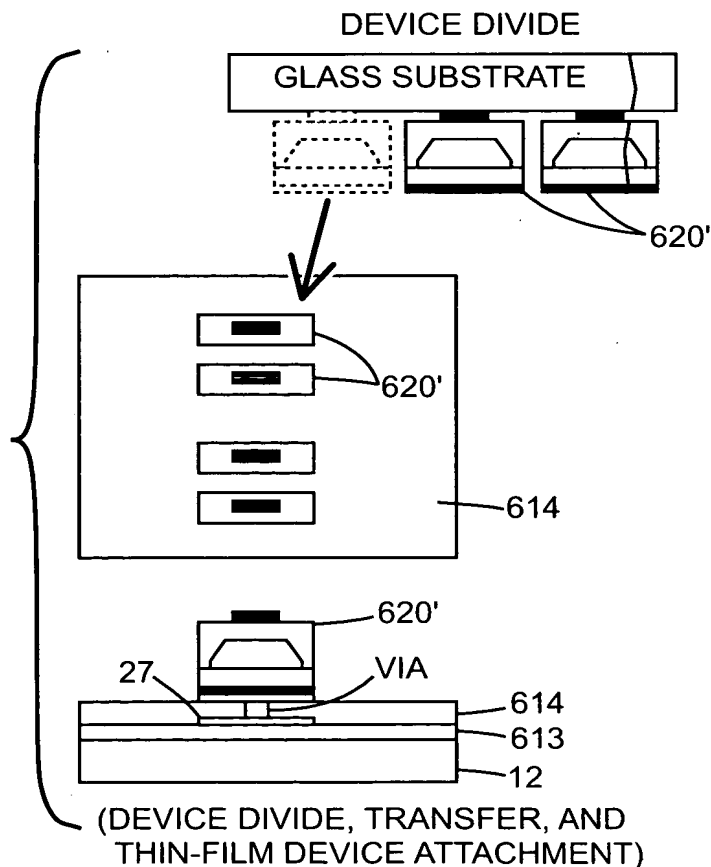


FIG. 84

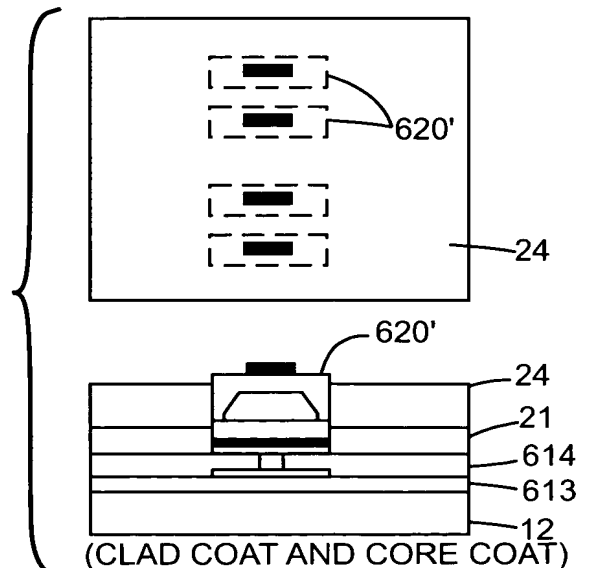
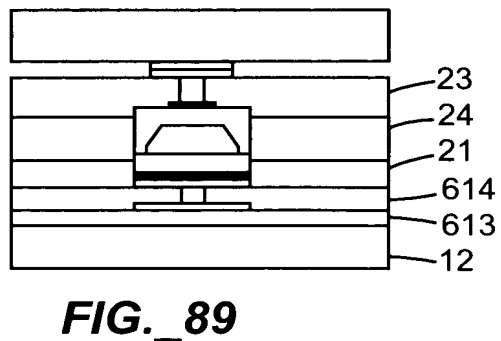
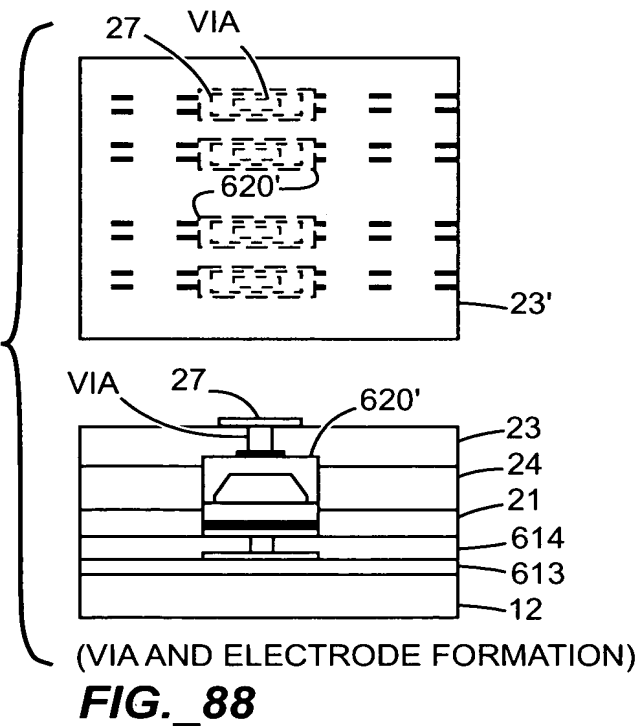
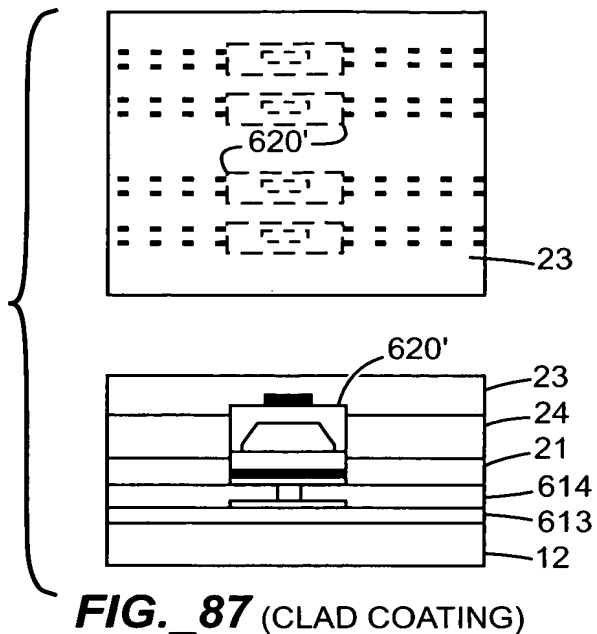
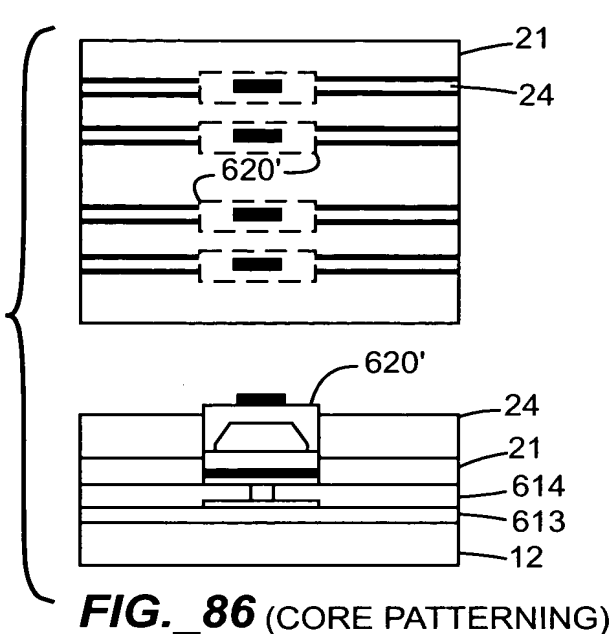
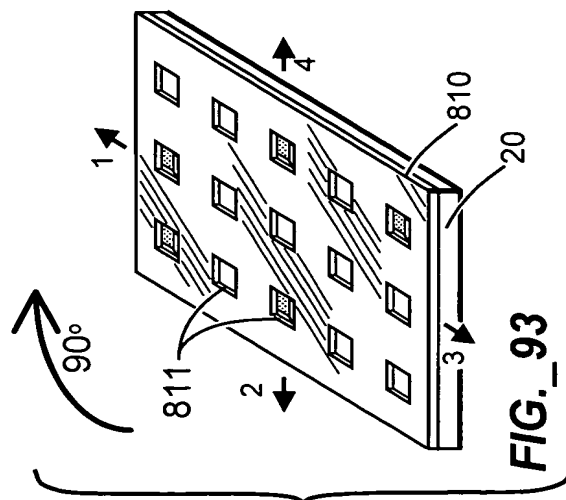
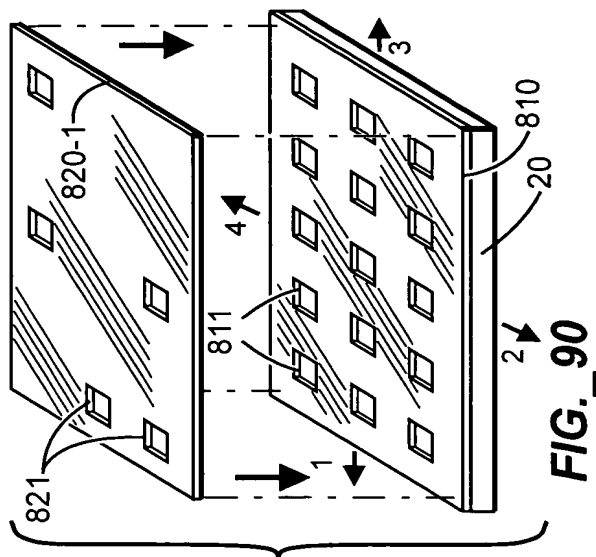
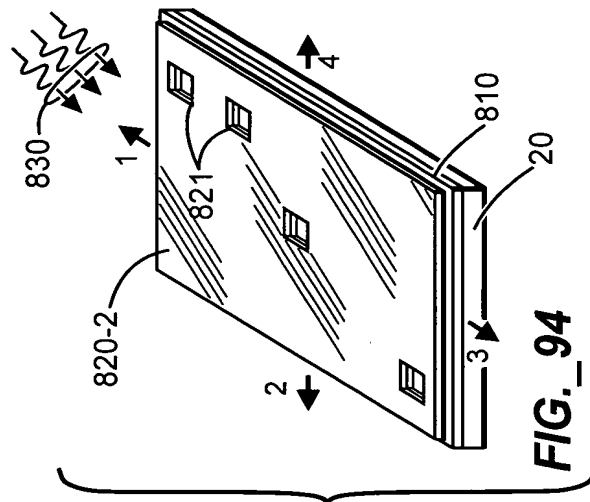
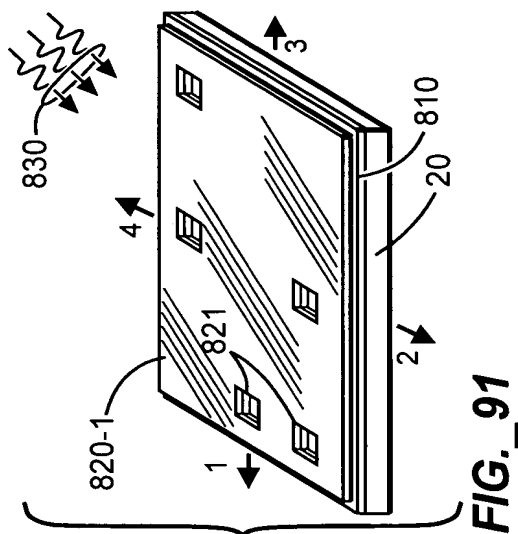
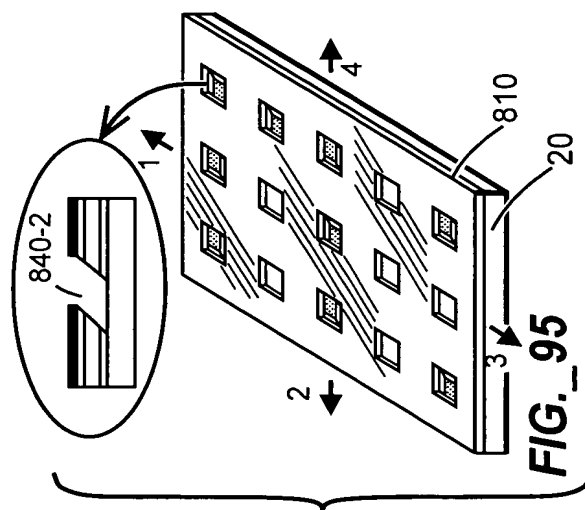
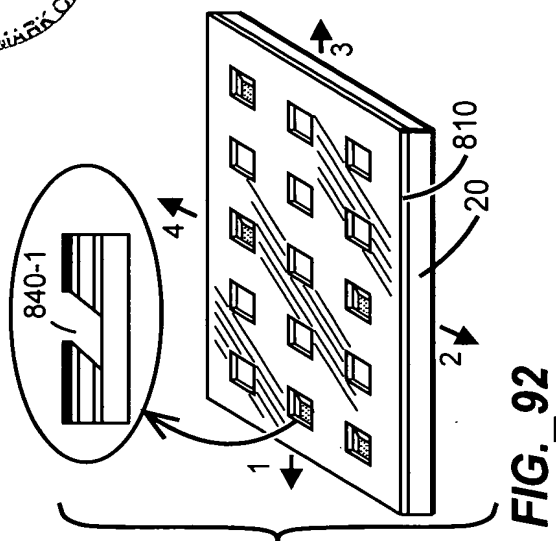
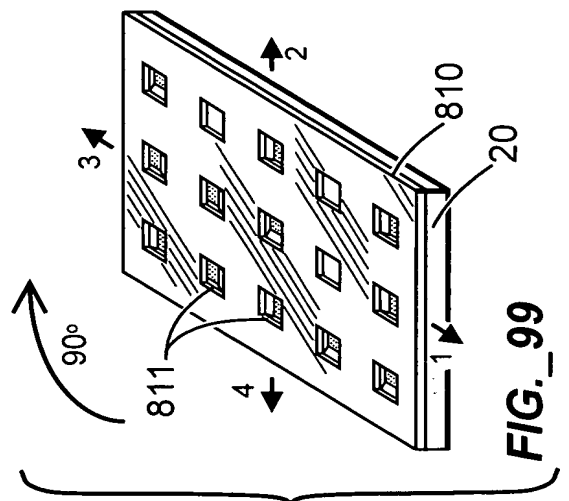
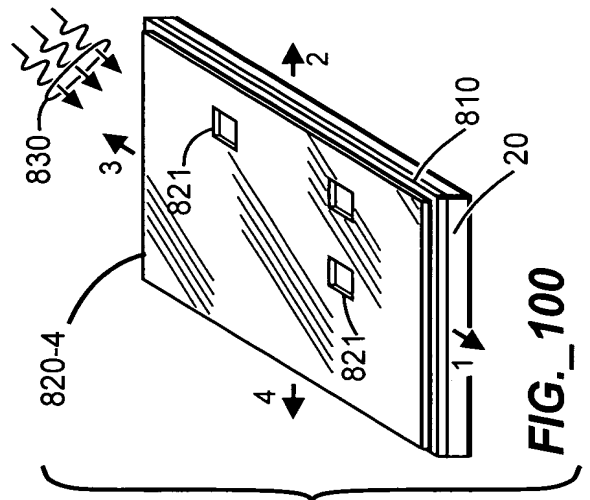
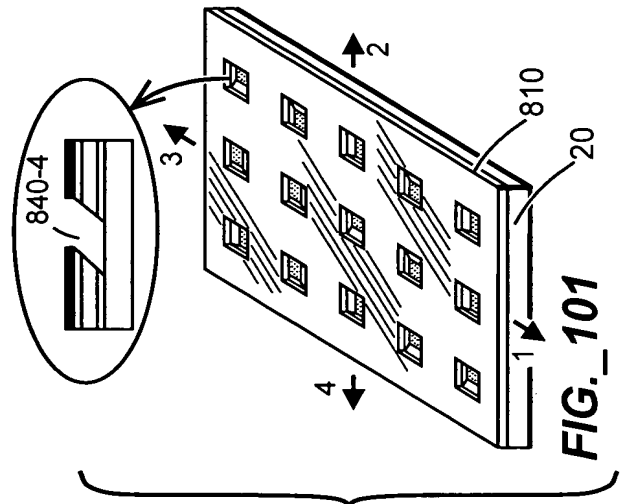
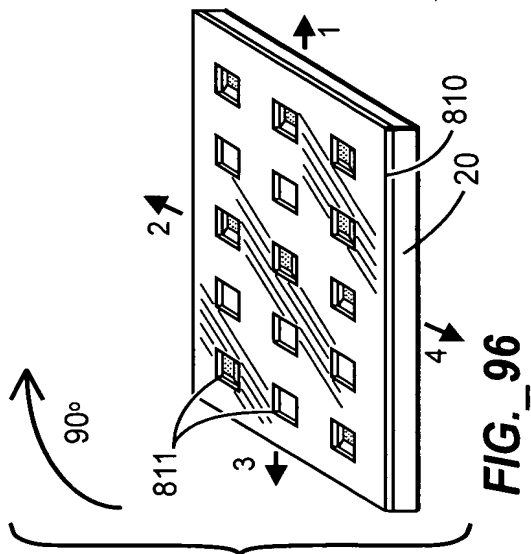
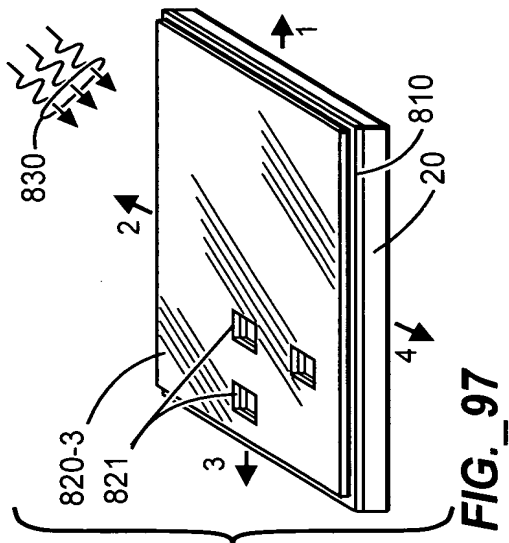
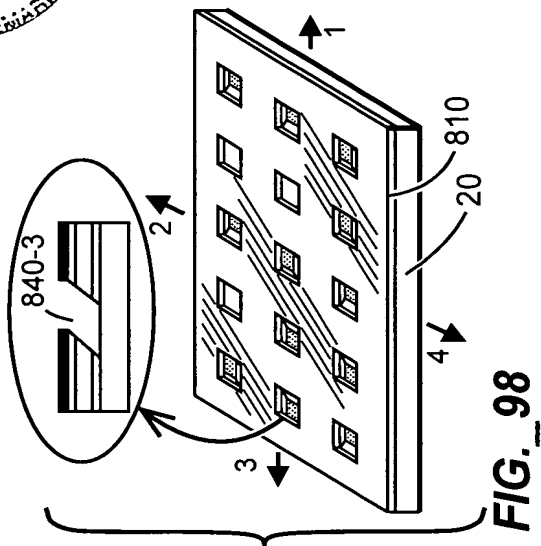


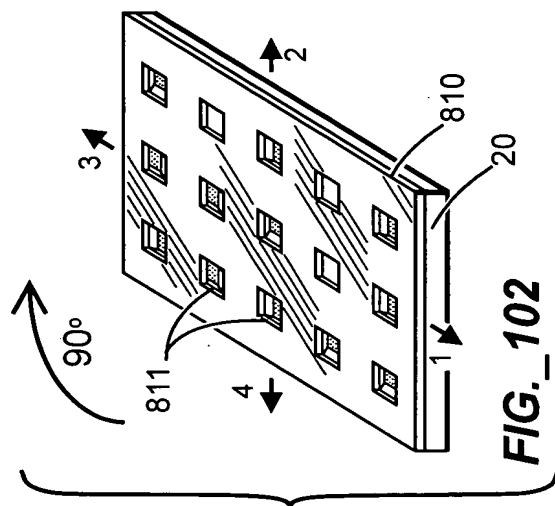
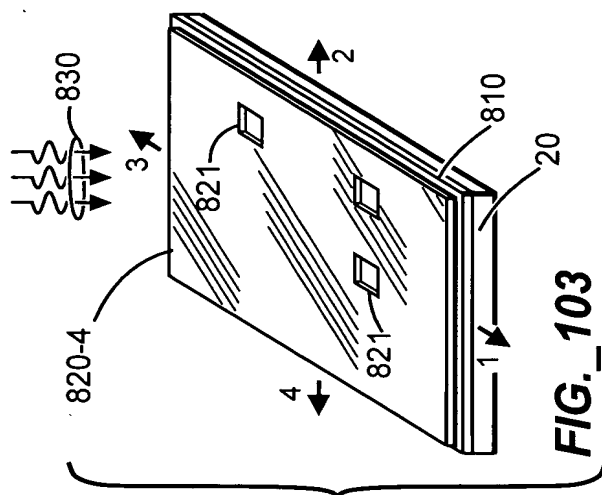
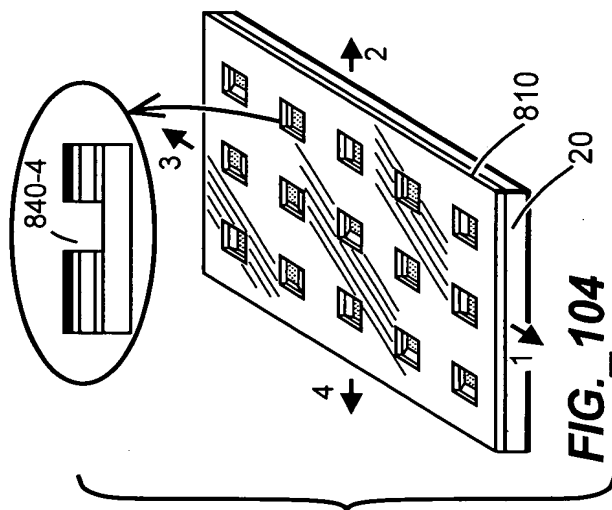
FIG. 85







37 / 61



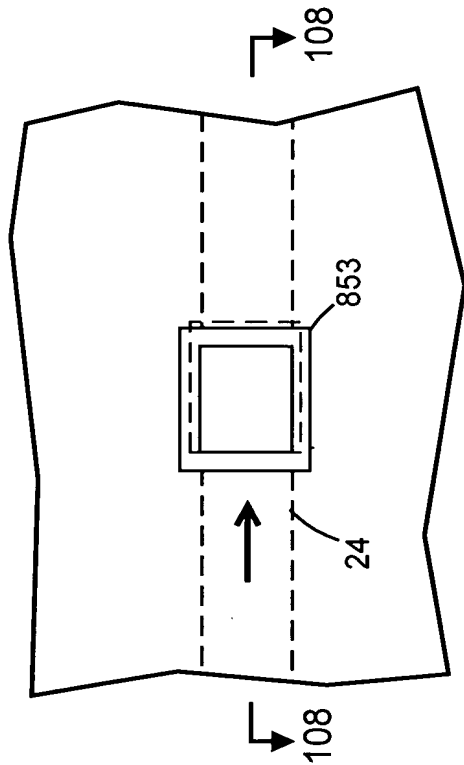


FIG. 107

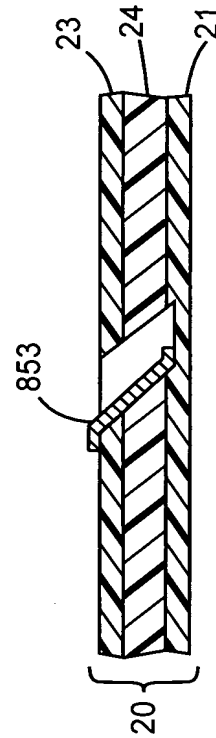


FIG. 108

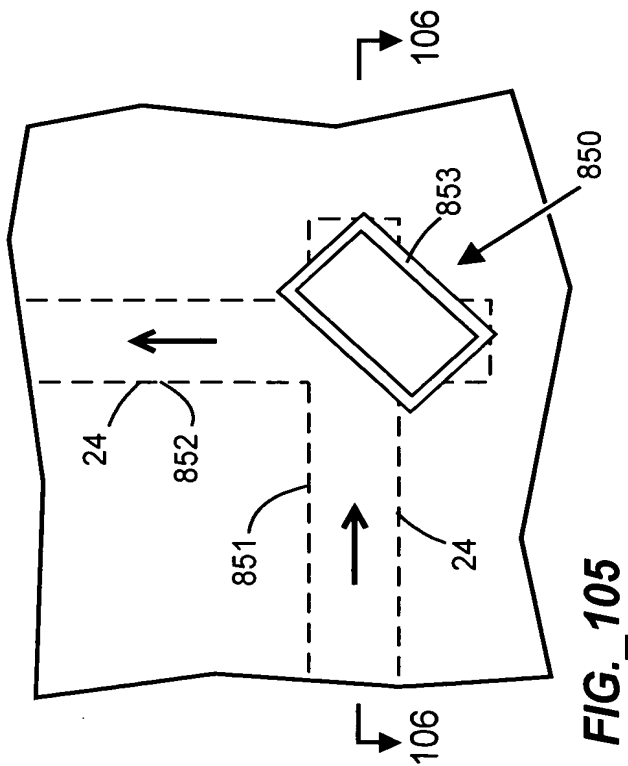


FIG. 105

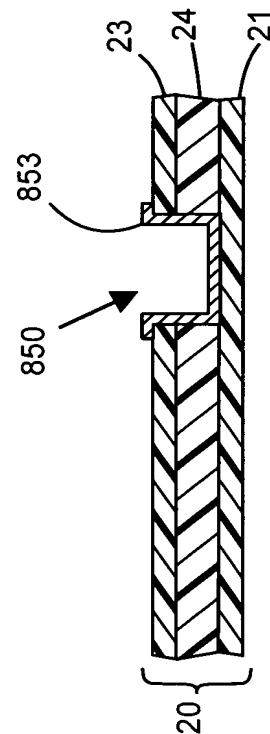
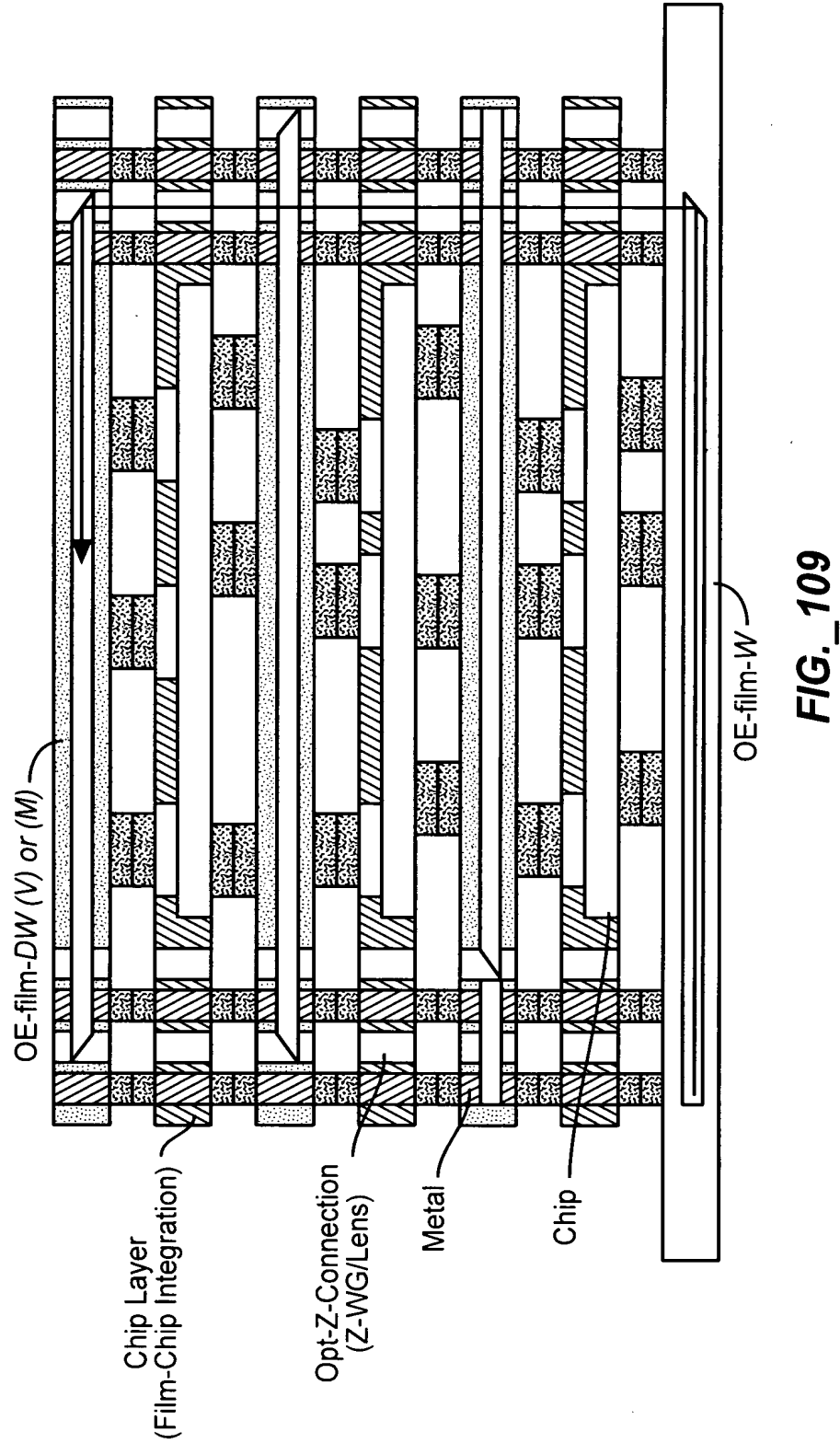
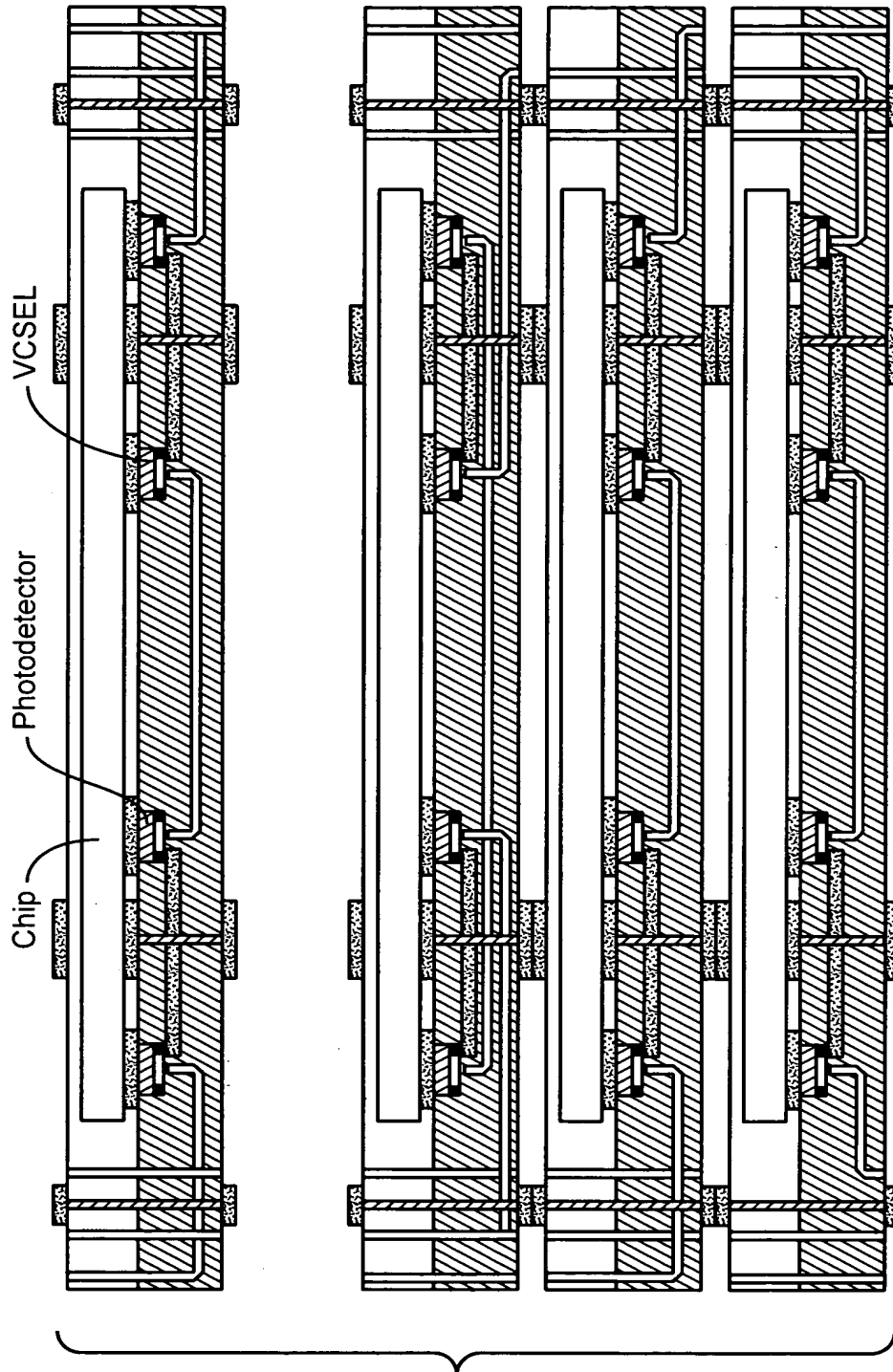


FIG. 106





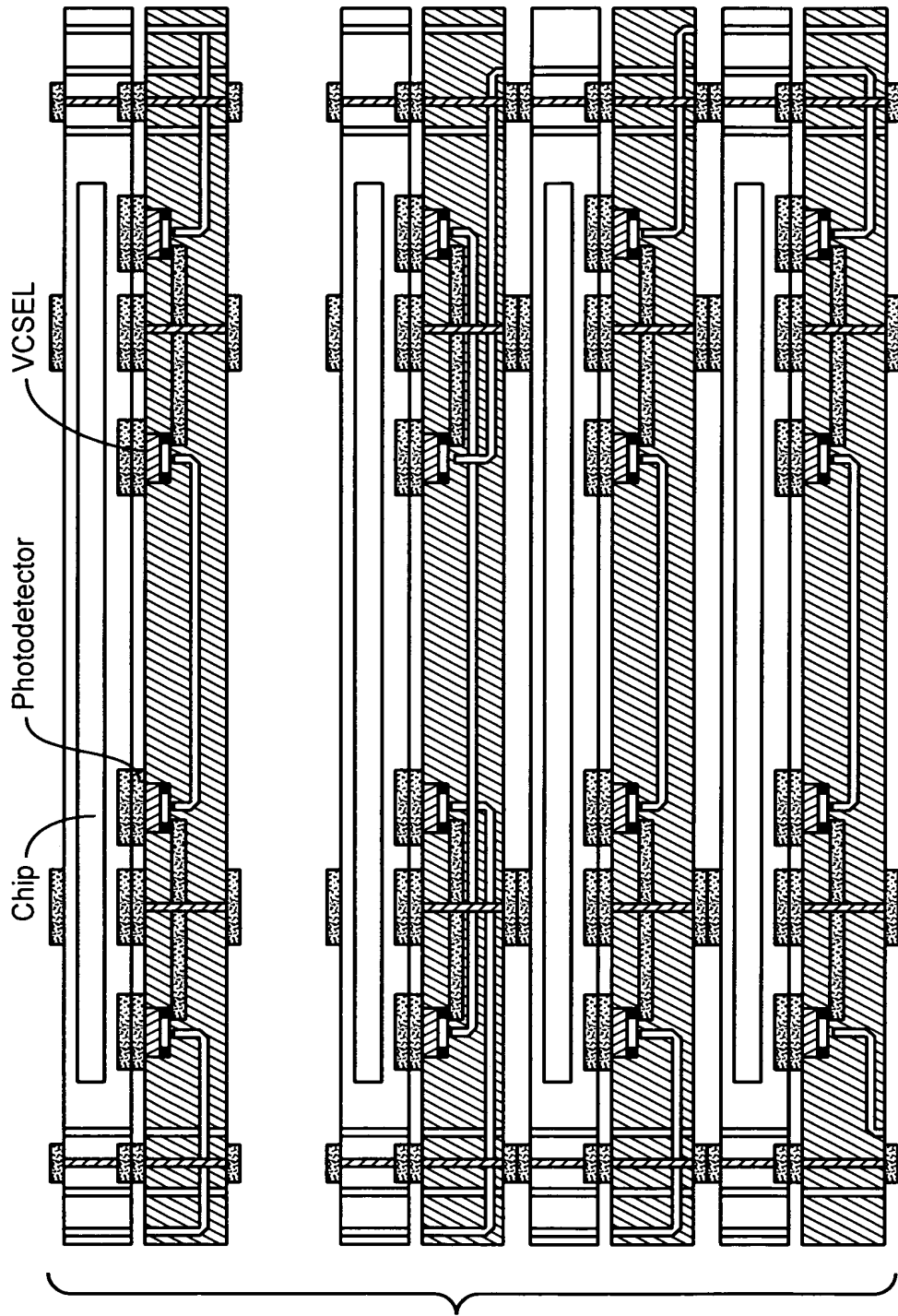


FIG._111

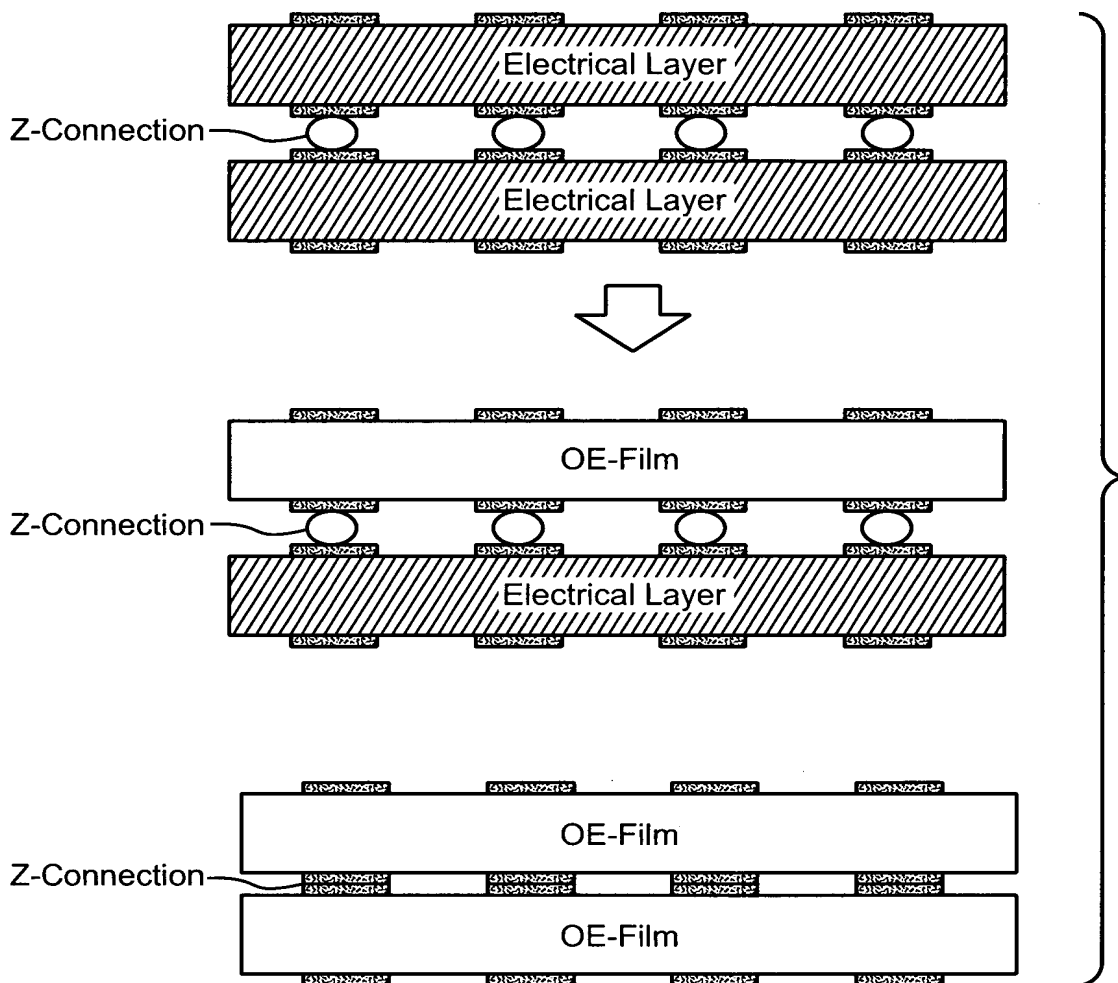
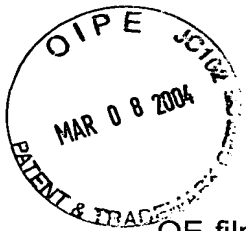


FIG._112



43 / 61

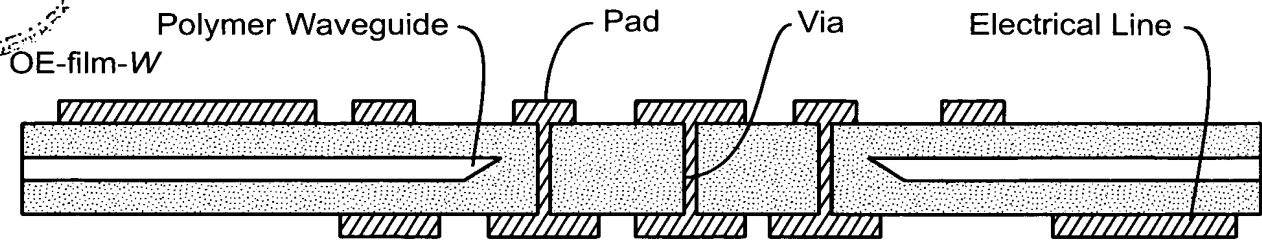


FIG._113

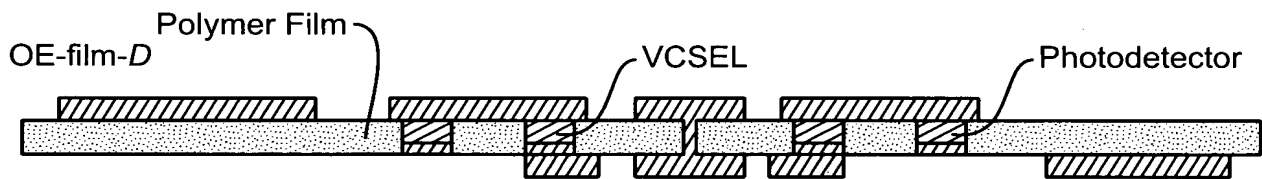


FIG._114

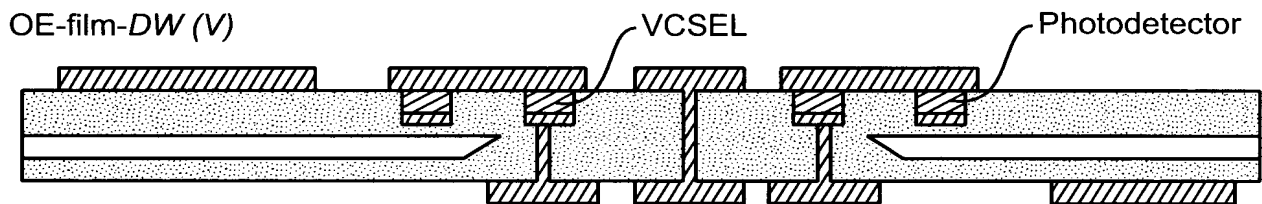


FIG._115

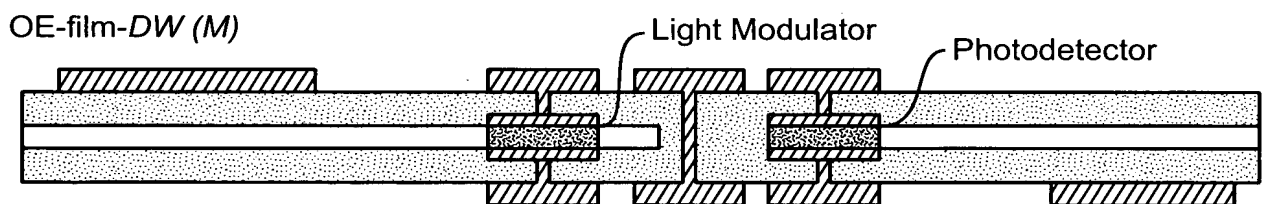


FIG._116



44 / 61

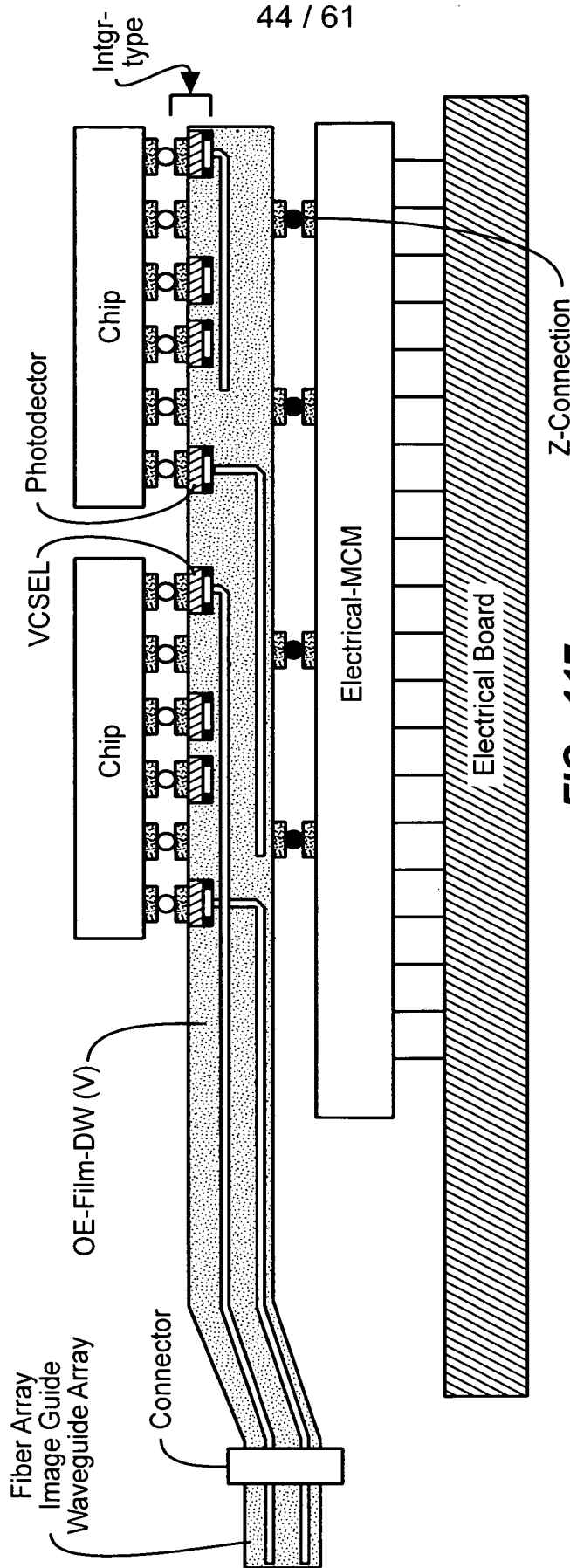


FIG. 117



45 / 61

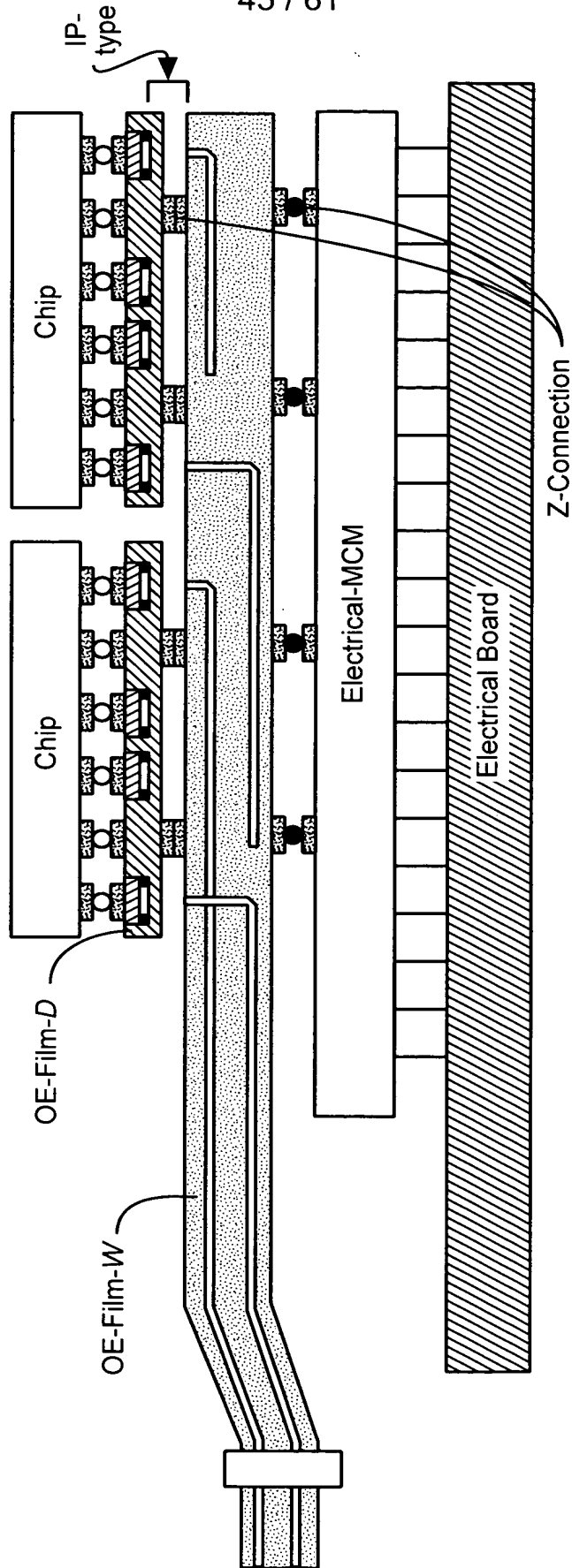


FIG. 118

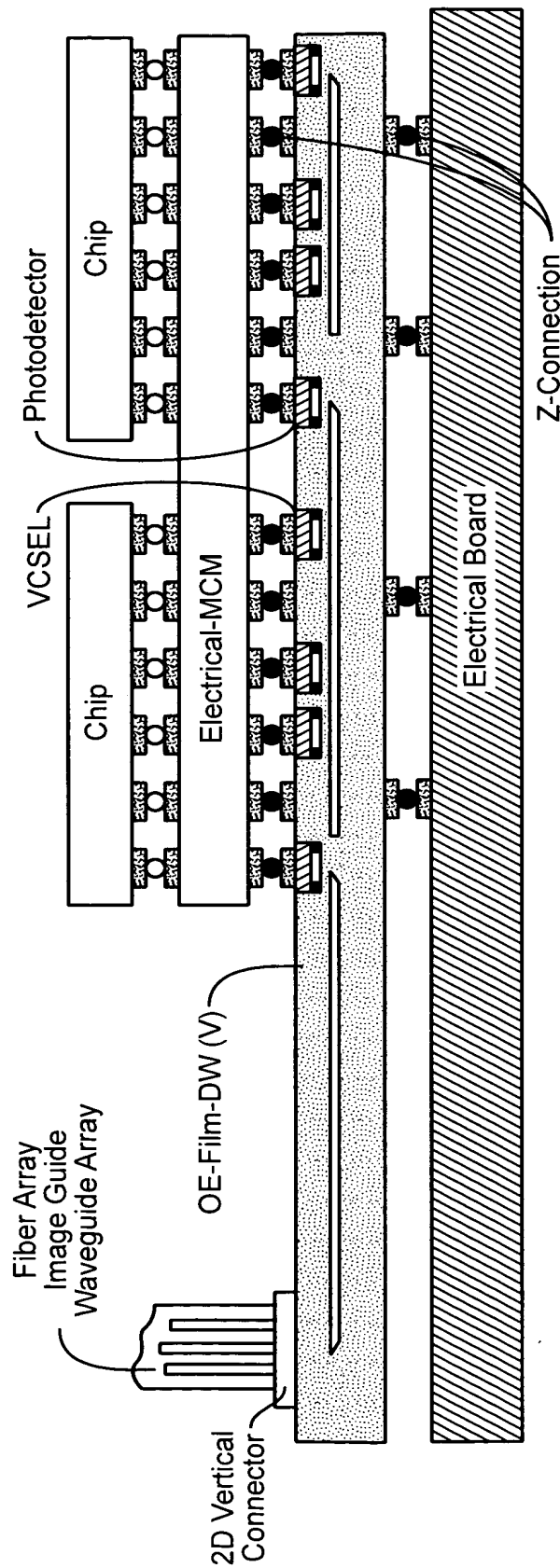


FIG. 119



"Multi-Layer Opto-Electronic Substrates with Electrical and Optical Interconnections and Methods for Making"

Inventors: Tetsuzo Yoshimura, et al.

Application Serial No.: 09/295,431

47 / 61

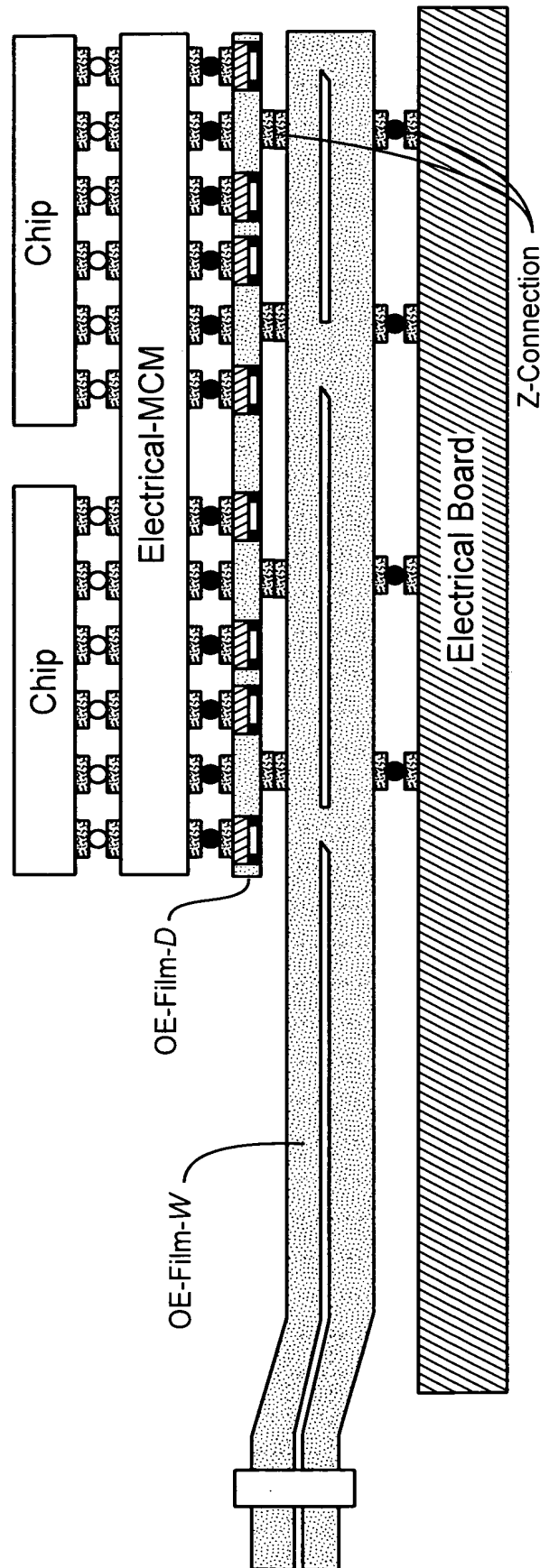


FIG._120

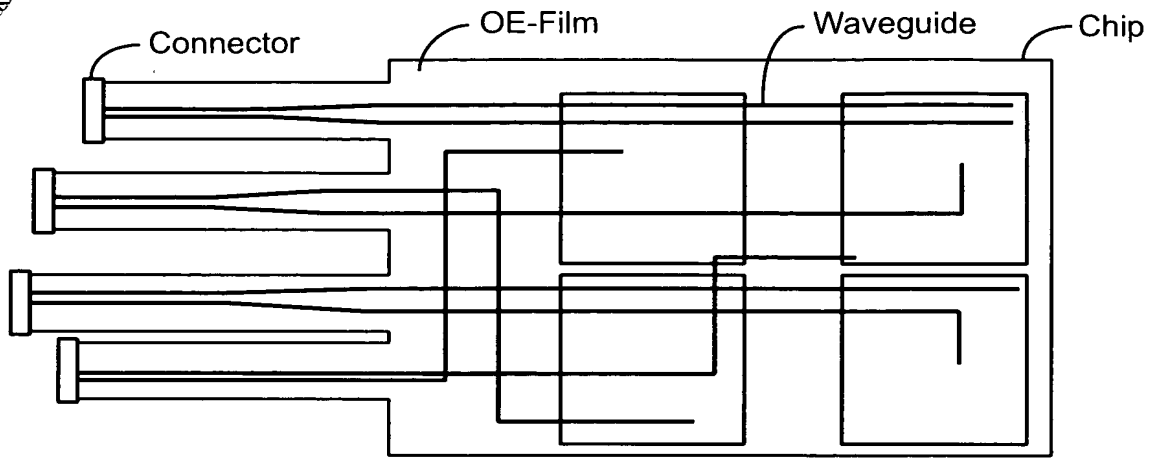


FIG. 121

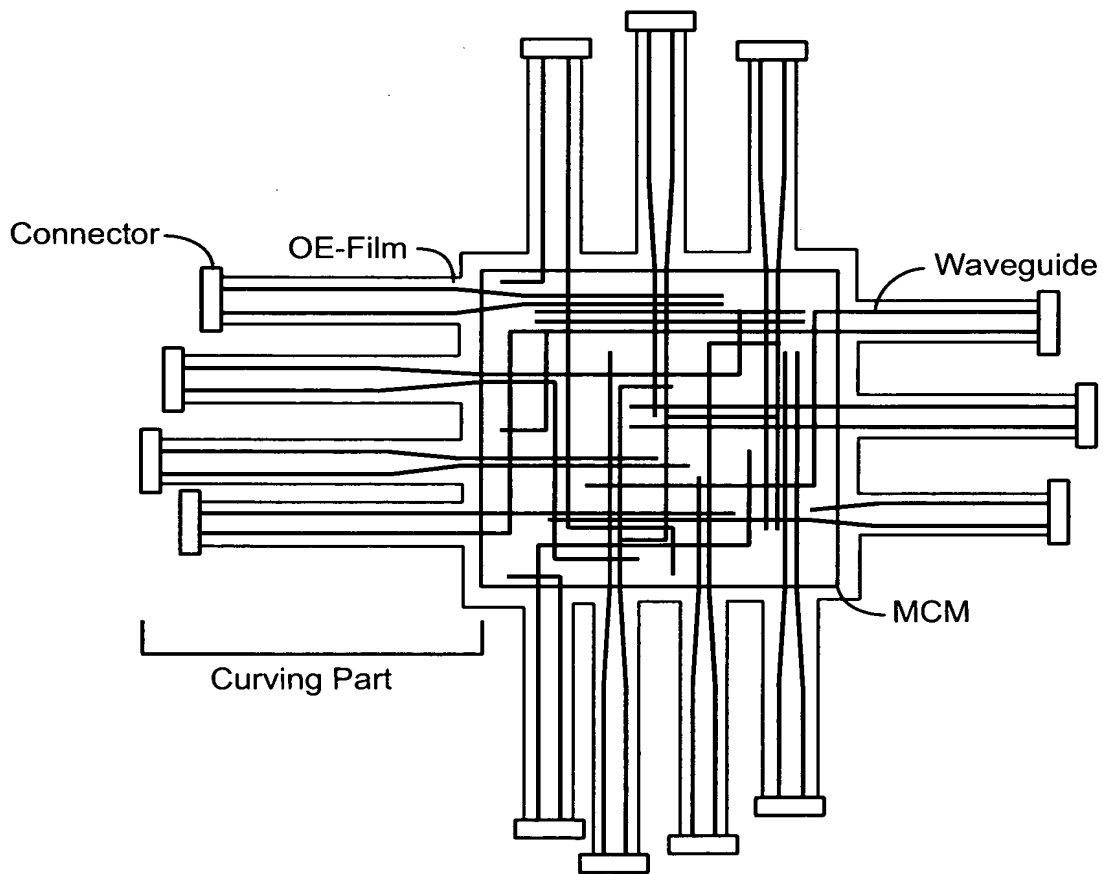


FIG. 122



49 / 61

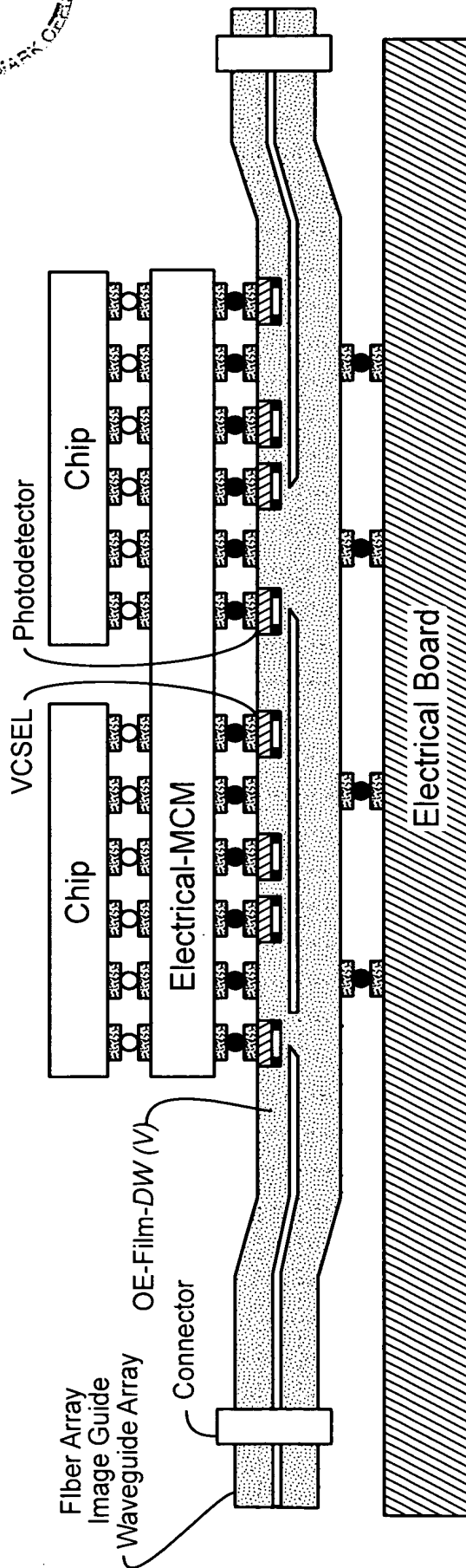


FIG. 123

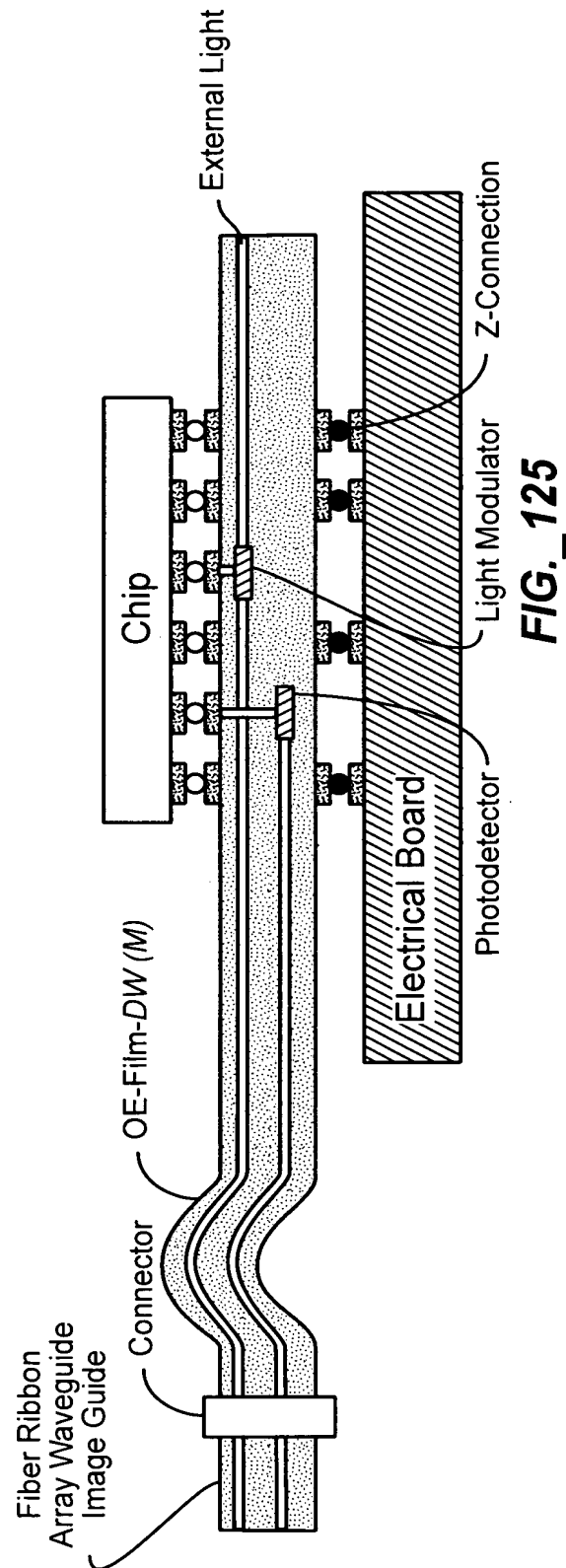


FIG. 125

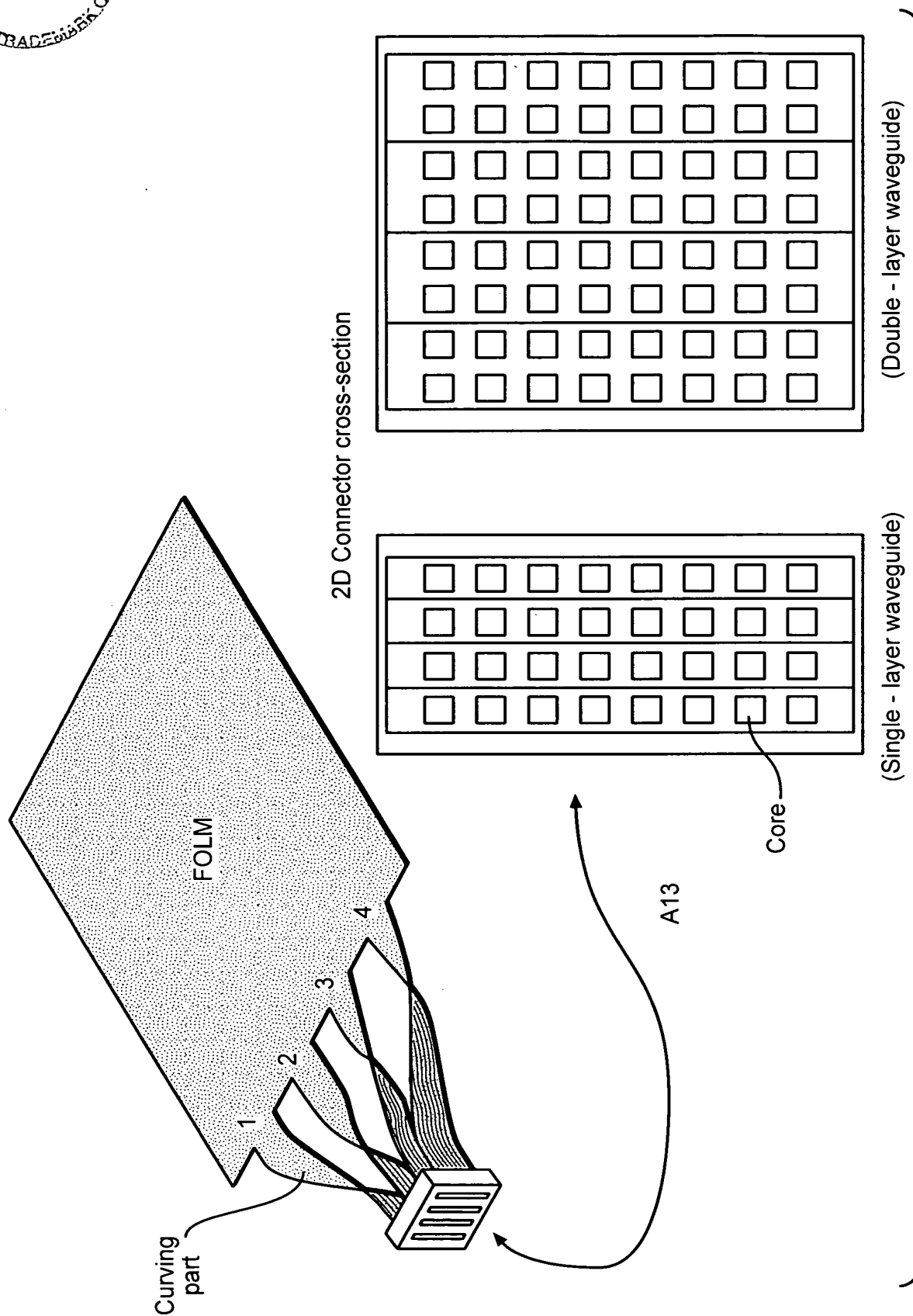
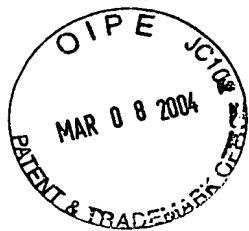


FIG. 124

FIG. 127



FIG._129

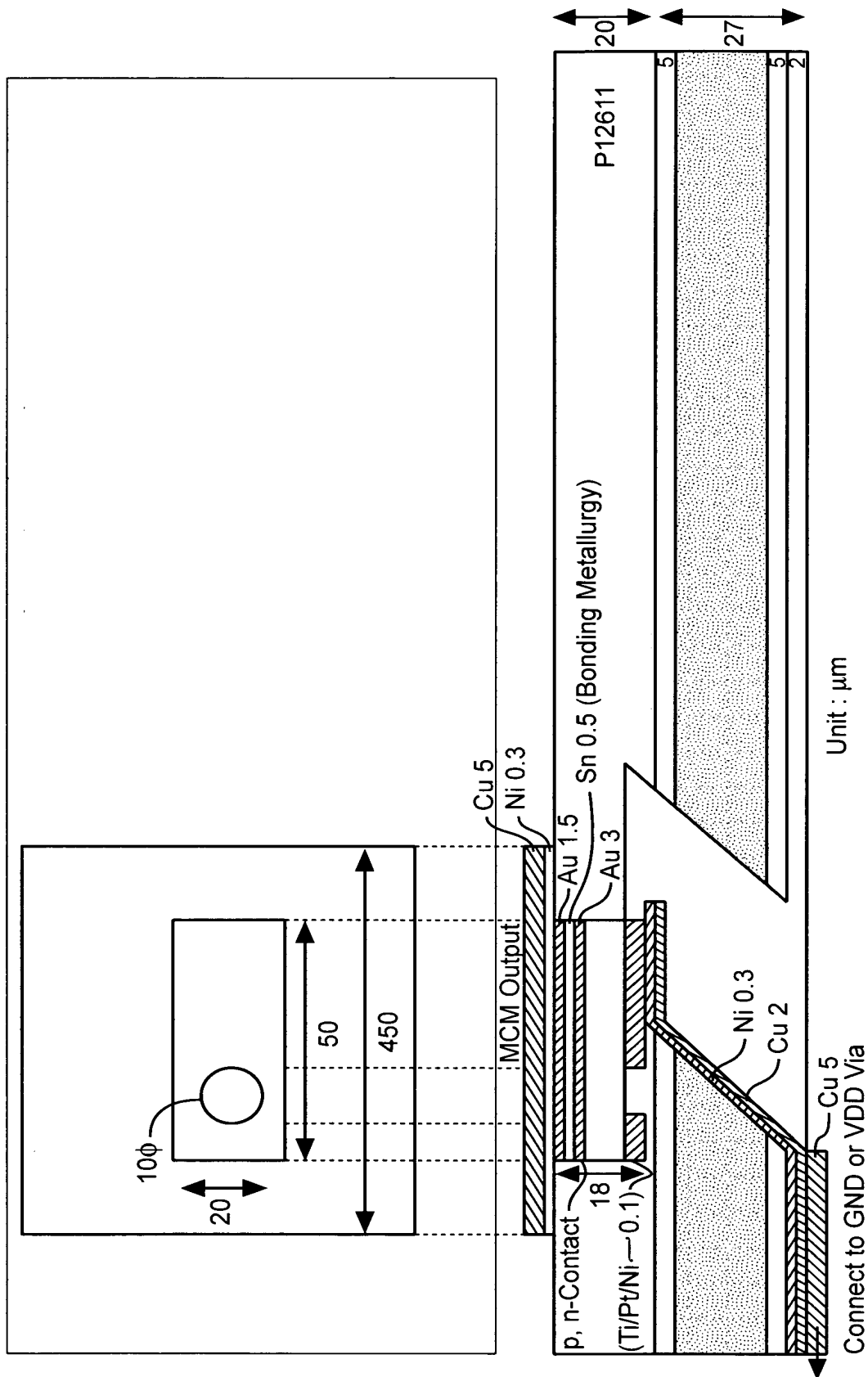


FIG._128

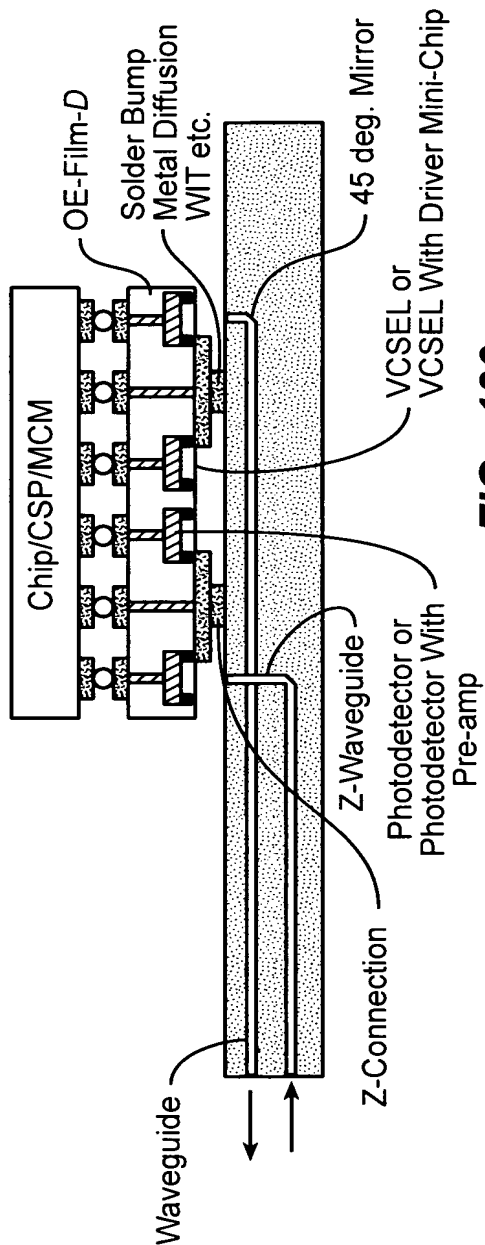


FIG. 130

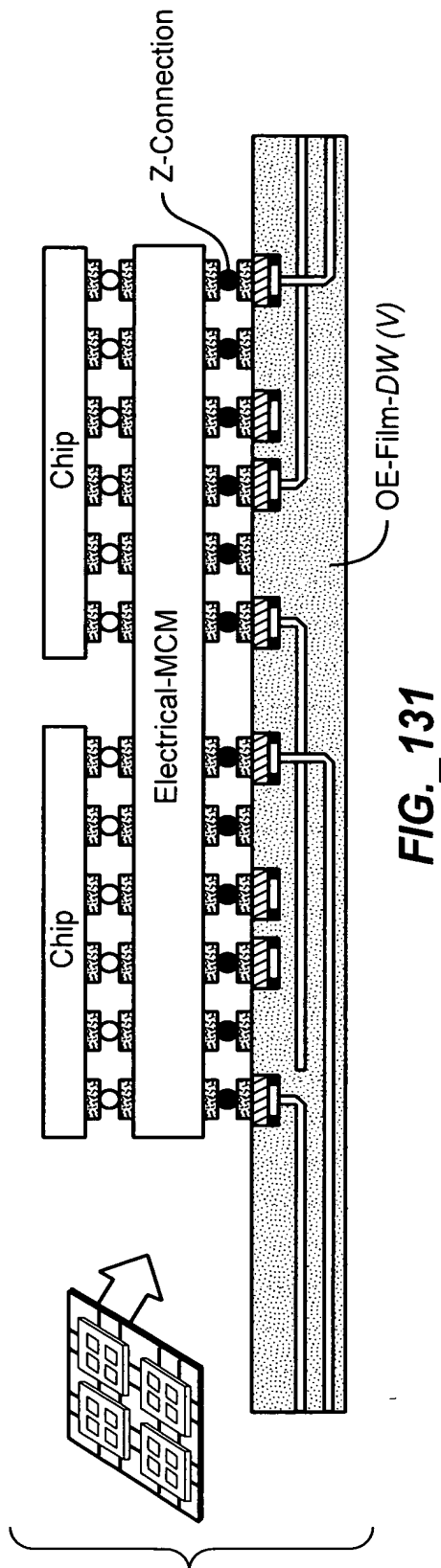


FIG. 131

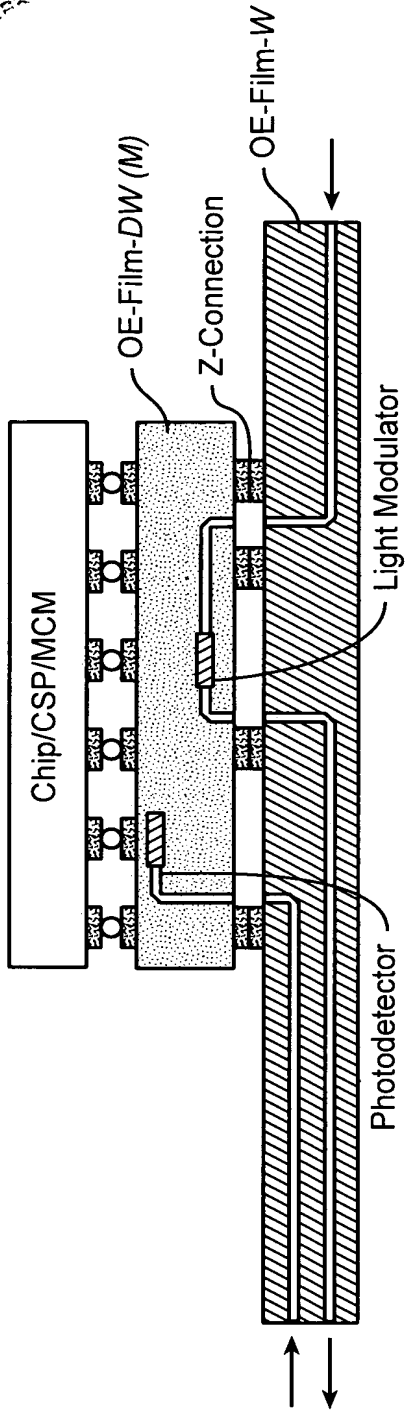


FIG._132

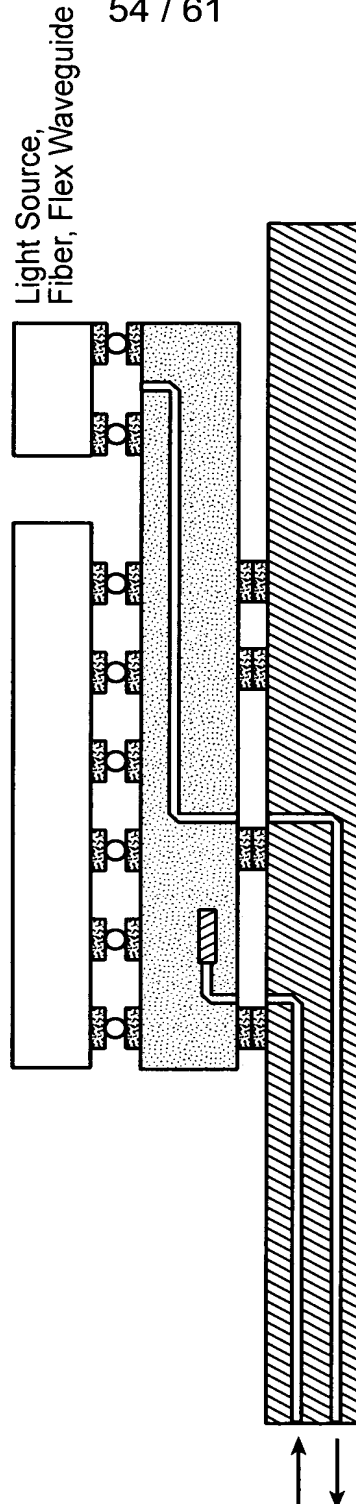


FIG._133

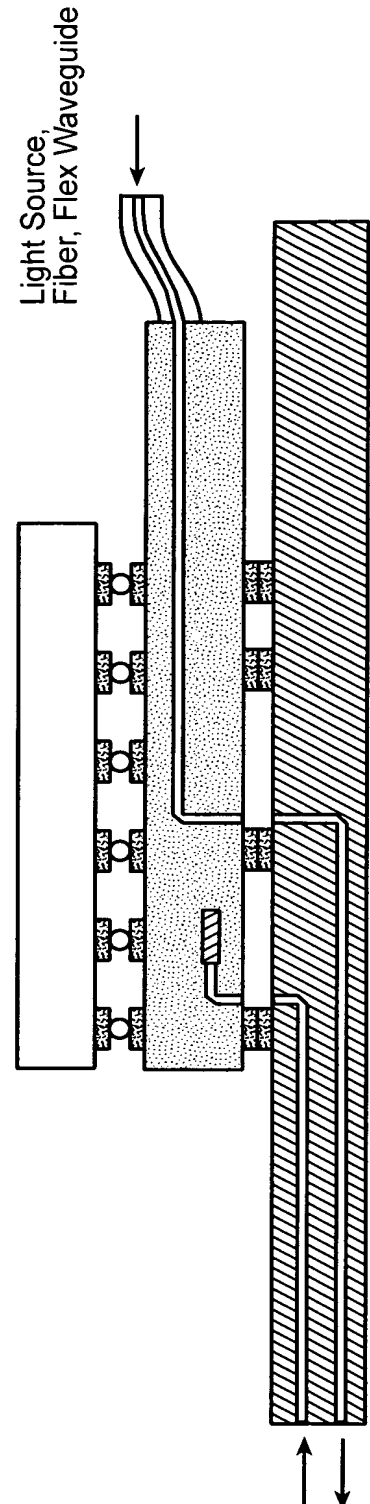
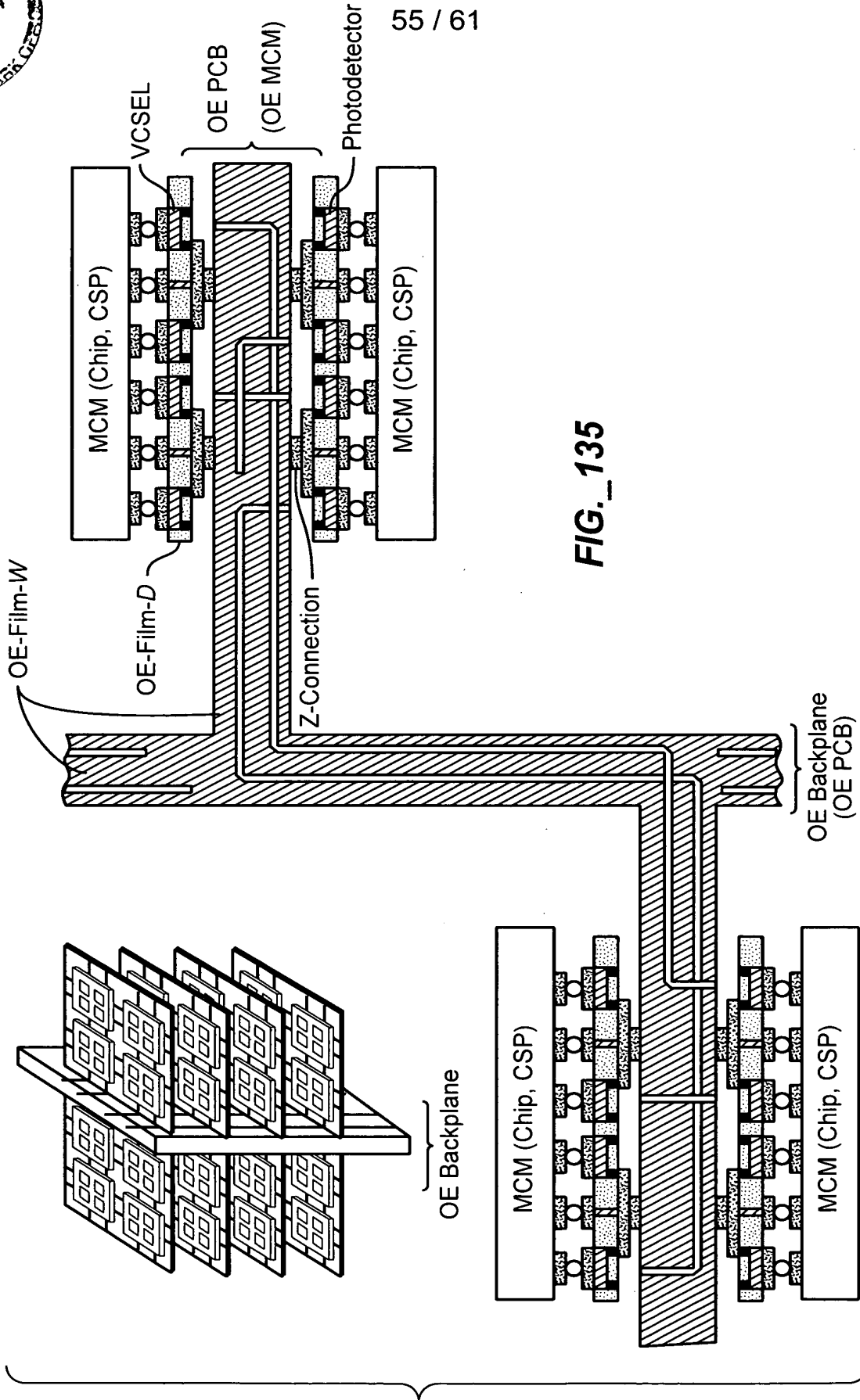


FIG._134



55 / 61





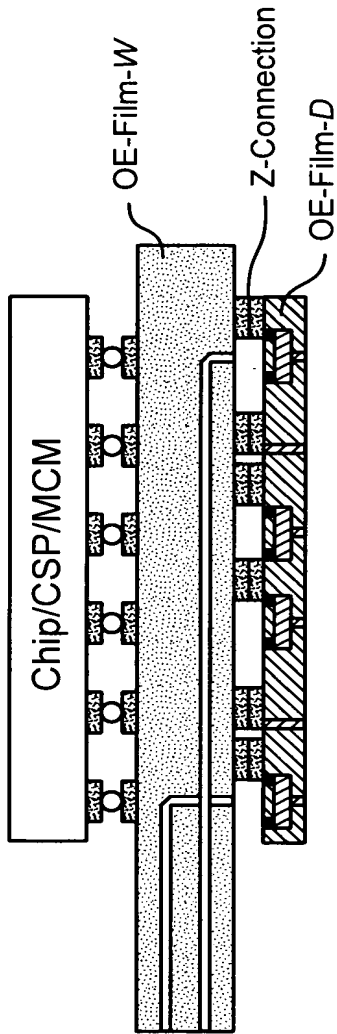


FIG._138

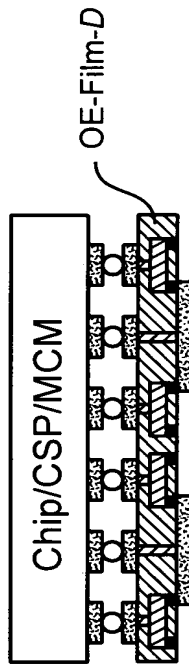


FIG._141

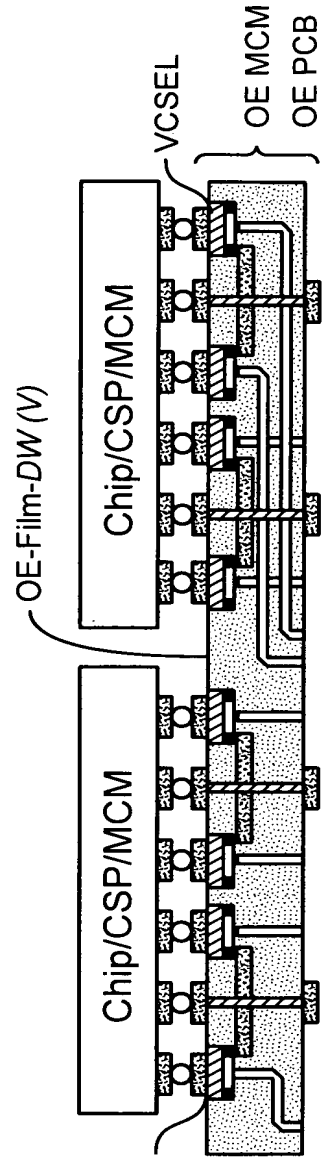


FIG._142

Photodetector

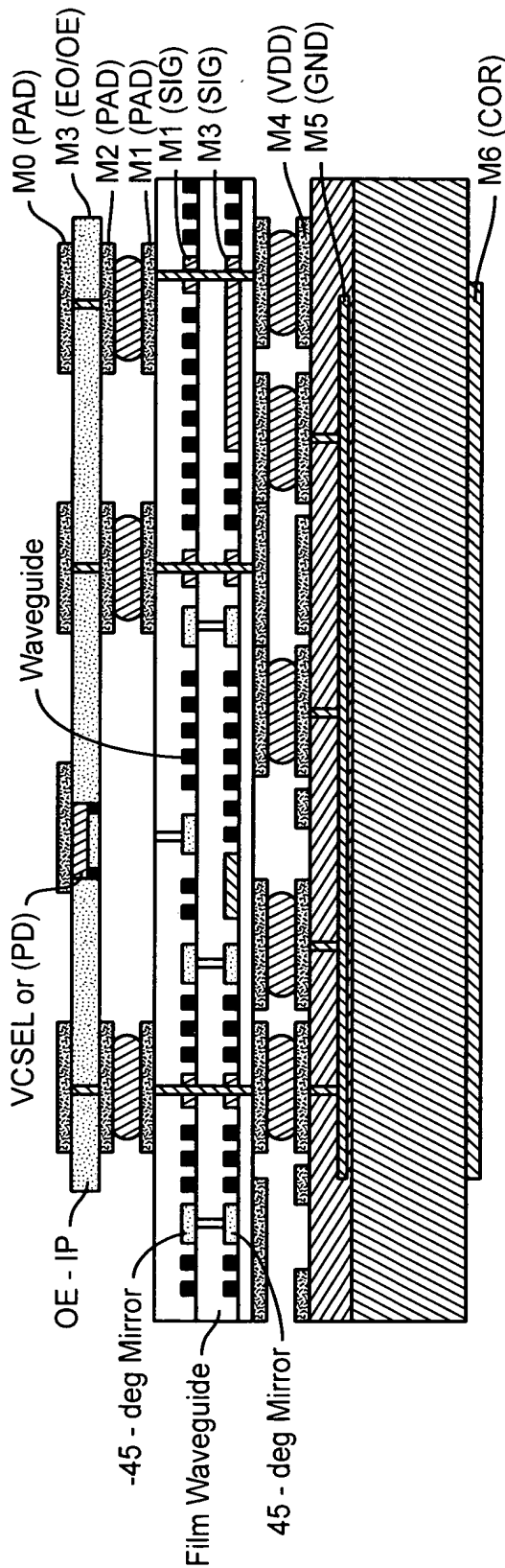


FIG. 139

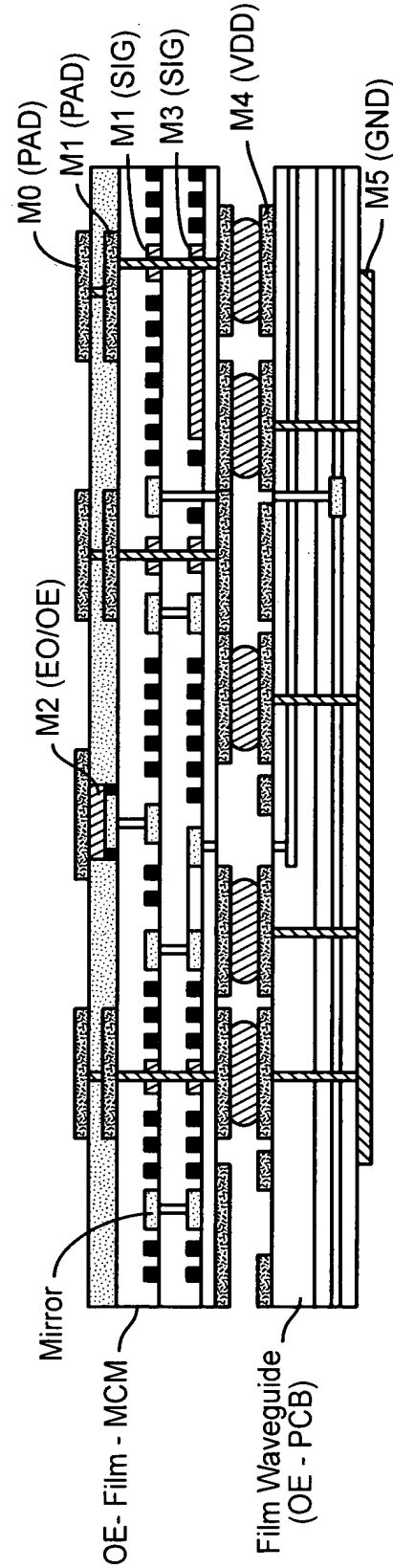
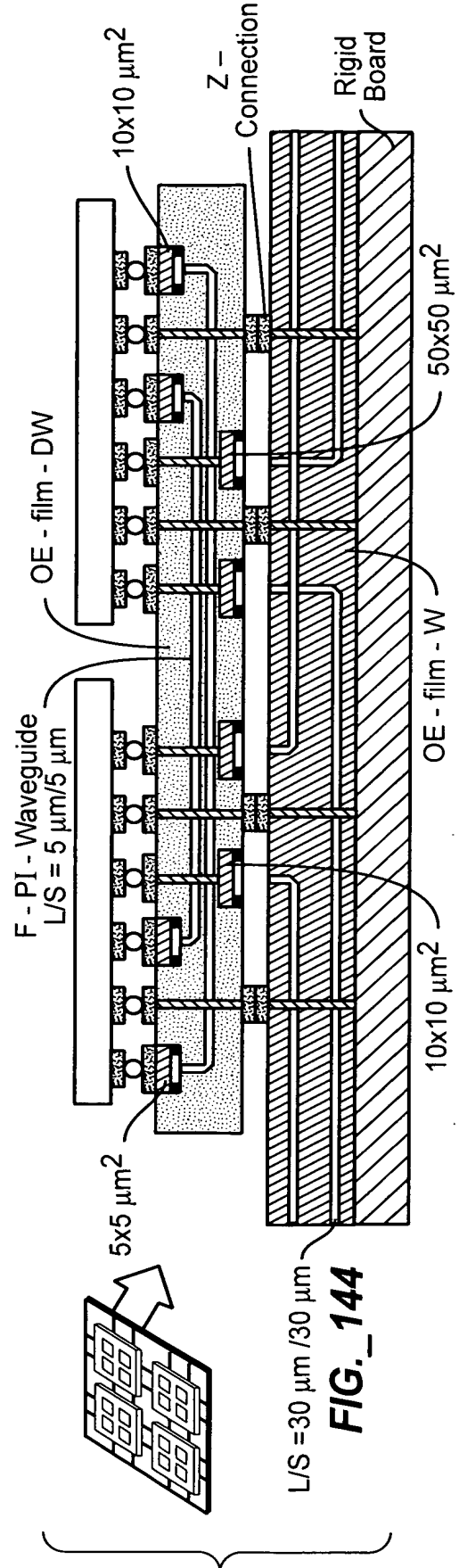
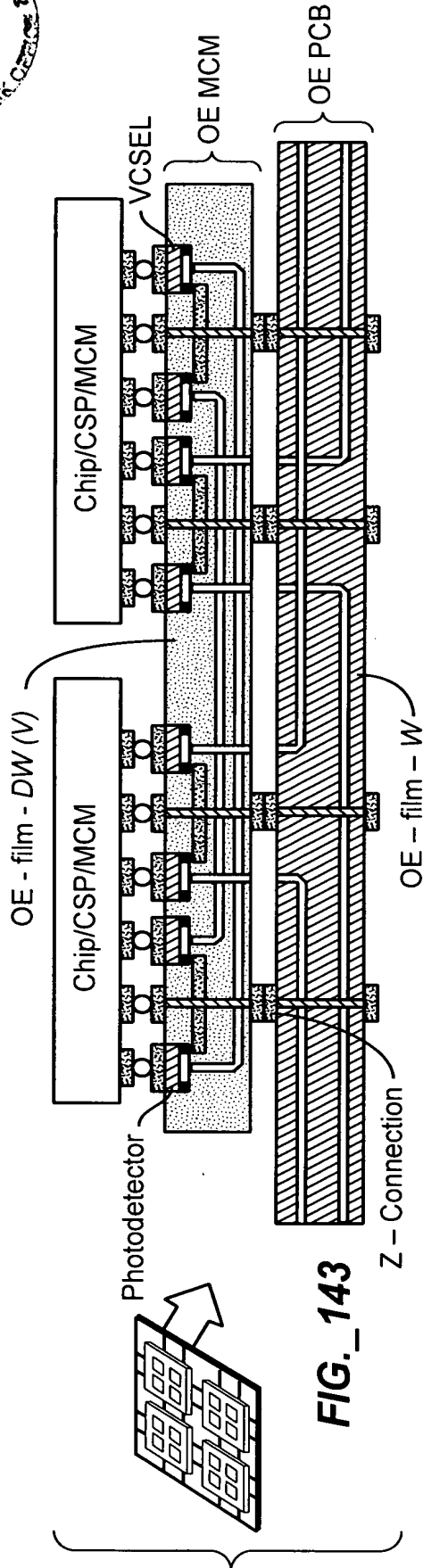
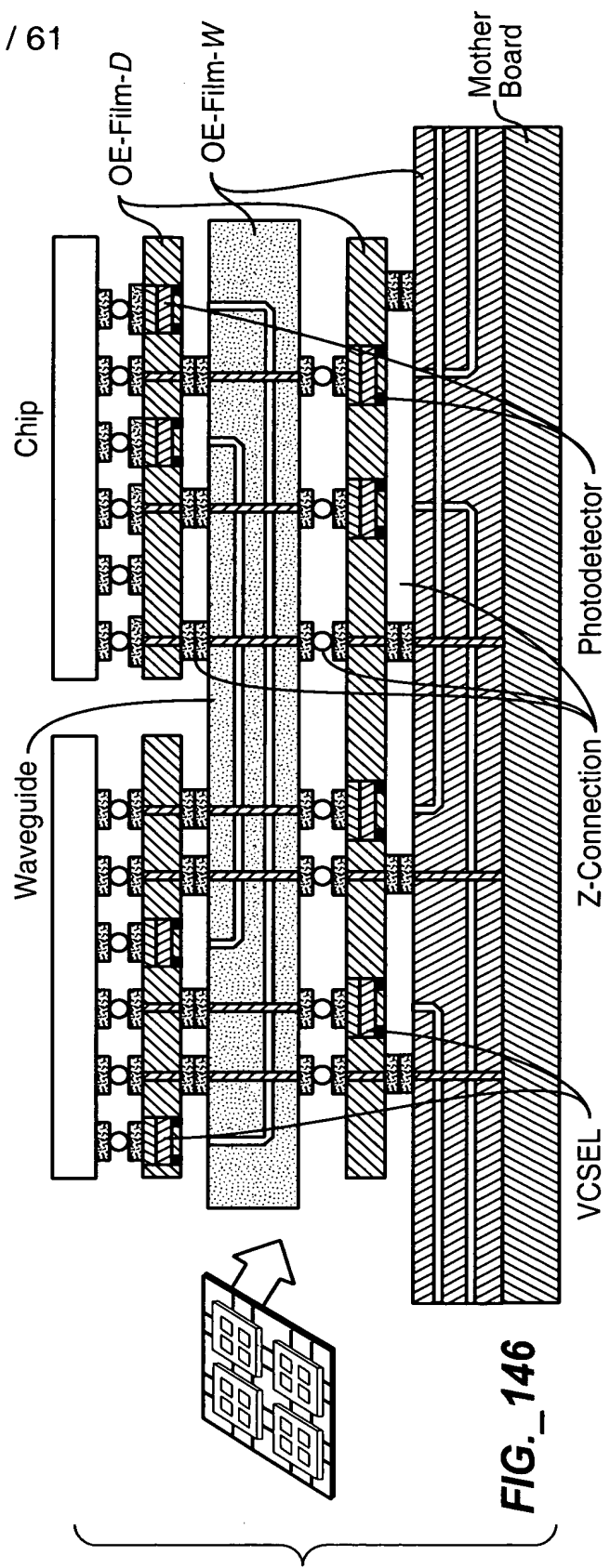
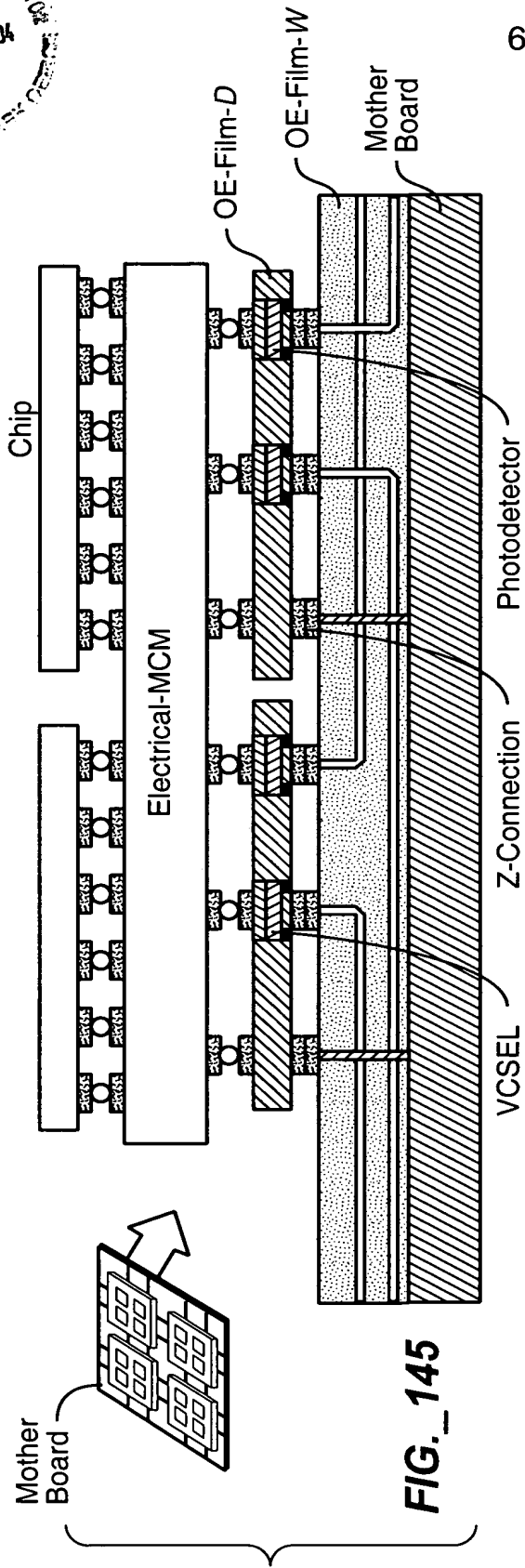


FIG. 140





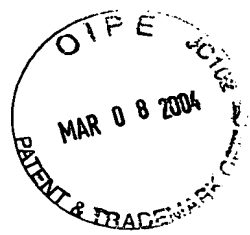


FIG._147

(PADS/LINES FORMATION)

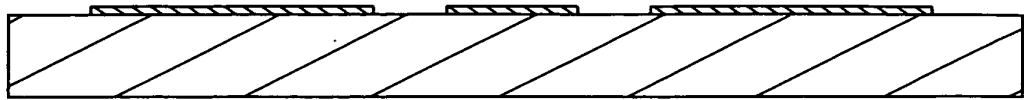


FIG._148

(PLACEMENT OF THIN-FILM DEVICES)

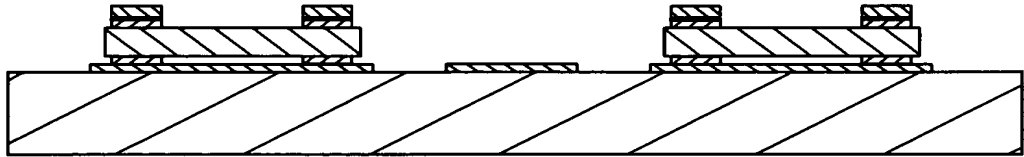


FIG._149

(POLYMER COAT)

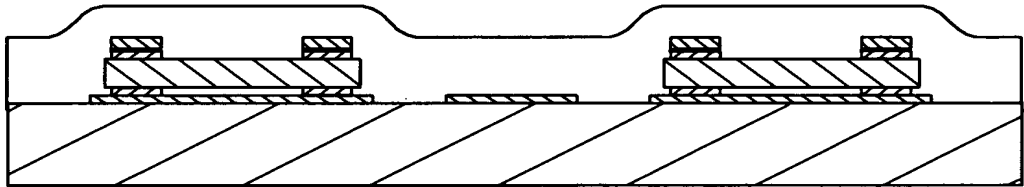


FIG._150

(PLANARIZATION)

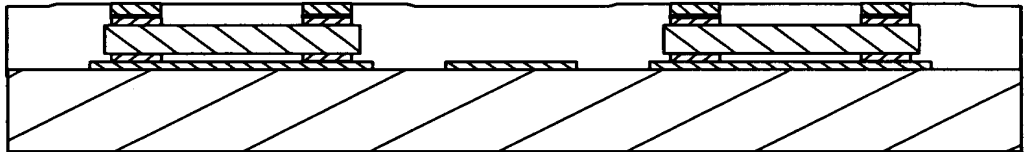


FIG._151

(VIAS/PADS/LINES FORMATION)

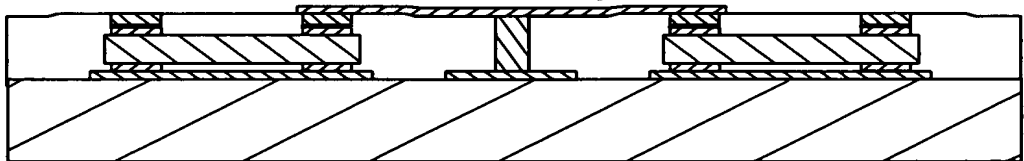


FIG._152

(SUBSTRATE REMOVAL)



FIG._153

(WAVEGUIDE FORMATION)

